

## SYD8821: Ultra Low Power Bluetooth 4.2 Single Mode SoC

### 1.1 General Description

The SYD8821 is a low power and high performance 2.4GHz Bluetooth Low Energy SoC. SYD8821 integrates all Bluetooth smart devices needed: a 32-bit ARM Cortex-M0 with Flash memory, digital interface and 2.4GHz RF transceiver. SYD8821 also integrates DCDC converter to provide SoC solution for stand-alone application as HID, Wearable Device.

### 1.2 Key Features

- Fully qualified Bluetooth low energy 4.2 Master/Slave device
- Cortex M0 32-bit MCU with max. 64MHz clock rate (8,16, 32 and 64MHz for optional)
- Low power and excellent performance 2.4GHz transceiver built-in balun for compact layout area
- Integrate 4Mb Flash, 128kB ROM and 192kB RAM, 16kB Cache RAM
- 8 channel 10-Bit 1Msps SAR ADC
- Integrate 32MHz and 32.768kHz XTAL oscillators
- Built in 64MHz and 32.768kHz RCOSC
- Communication interface options
- I2C(Master)x2; I2C(Slave)x1
- 2-Wire SPI(Master); 4-Wire SPI(Master);
- UART x2
- Digital peripherals
- LED x3
- PWM x12 (3x4)
- Support Serial Wire (SW) debug mode
- Integrate Quadrature Decoder

- Capacitance detection for key applications.
- Keyboard Scanner
- Integrated DCDC converter
- Operating Temperature: -40 ~85°C

### 1.3 Applications

- Wearable device (wristband, smart watch, etc.)
- HID device (smart remote controller, etc.)
- BLE module (UART transmission)
- Health applications (smart weight, etc.)
- Home and industrial automation

### 1.4 Key Parameters

Parameter	Value
Max TX Power	4 dBm
RX Sensitivity	-94 dBm
TX RF Current @0dBm	4.2 mA
*Vbat=3V, on-chip DCDC	
RX Current @sensitivity	2.4 mA
*Vbat=3V, on-chip DCDC	
Sleep Mode Current	2.5 uA
Deep Sleep Mode Current	1 uA
RF Input Impedance	50 Ω
Internal Flash	512 kB
SRAM	192 kB
BAT Supply Voltage (V)	1.7~4.3V
GPIO	31
Operating Temperature, Tj	-40~+85 °C

**MENU**

SYD8821: Ultra Low Power Bluetooth 4.2 Single Mode SoC .....	1
1.1 General Description .....	1
1.2 Key Features.....	1
1.3 Applications.....	1
1.4 Key Parameters .....	1
2.0      Introduction .....	6
2.1 Overview .....	6
3.0      Pin assignments .....	8
4.0      Absolute maximum ratings .....	13
5.0      Recommended operating conditions.....	15
6.0      Mechanical specifications .....	16
7.0      CPU.....	17
8.0      Memory.....	18
9.0      Peripheral interface.....	21
10.0     Debugger interface (DIF).....	22
10.1     Trace pin multiplexing .....	23
11.0     Power management (POWER) .....	25
11.1     Main regulators.....	26
11.2     LDO regulator setup.....	27
11.3     DC/DC converter setup .....	27
11.4     System OFF mode .....	29
11.5     System ON mode.....	30
11.6     Sub power modes .....	30
11.7     Power supply supervisor.....	33
11.8     Power-fail comparator .....	33
11.9     RAM blocks.....	34
11.10    Reset.....	34
11.11    Power-on reset.....	34
11.12    Pin reset .....	34
11.13    Wakeup from System OFF mode reset .....	35
11.14    Soft reset.....	35
11.15    Watchdog reset.....	35
11.16    Brown-out reset .....	35

11.17	Retained registers .....	35
11.18	Reset behavior .....	35
11.19	Power Management (SD: VPOF) .....	36
12.0	Clock management (CLOCK) .....	37
12.1	32MHz Crystal Oscillator .....	37
12.2	64MHz RC Oscillator.....	39
12.3	32.768kHz Crystal Oscillator .....	39
12.4	32.768kHz RC Oscillator .....	40
12.5	32.768 kHz synthesized from HFCLK (LFSYNT).....	40
12.6	External clock references .....	40
12.7	High Frequency clock references (2016.5.15 Add) .....	40
12.8	Calibrating the 32.768 kHz RC oscillator .....	40
13.0	General purpose input/output (GPIO).....	42
14.0	GPIO tasks and events (GPIOE) .....	43
15.0	2.4 GHz Radio (RADIO).....	44
15.1	General Radio Characteristics .....	44
15.2	Radio Current Consumption .....	44
15.3	Transmitter Specification .....	44
15.4	Receiver Specification .....	45
15.5	Radio Timing Parameters .....	46
15.6	RSSI Specifications.....	46
16.0	Timer/counter (TIMER) .....	48
17.0	Real time counter (RTC) .....	49
18.0	Random number generator (RNG).....	53
18.1	Bias correction .....	53
18.2	Speed .....	54
19.0	AES electronic codebook mode encryption (ECB) .....	55
19.1	DMA .....	55
19.2	ECB data structure .....	55
19.3	Shared resources.....	56
19.4	Electrical Specification .....	56
20.0	TX/RX FIFO depth .....	57
21.0	AES CCM mode encryption (CCM) .....	58
22.0	Accelerated address resolver (AAR).....	60

23.0	CMAC/ECDH .....	61
24.0	Serial peripheral interface master (SPIM) with DMA .....	62
25.0	SPI slave (SPIS).....	65
26.0	I2C compatible two-wire interface master with DMA.....	67
27.0	I2C compatible two-wire interface slave with DMA .....	71
28.0	Universal asynchronous receiver/transmitter with DMA (UARTE) .....	72
28.1	Functional description .....	73
28.2	Pin configuration .....	73
28.3	Shared resources.....	74
28.4	Transmission.....	74
28.5	Reception .....	75
28.6	Suspending the UART.....	76
28.7	Error conditions.....	76
28.8	Using the UART without flow control .....	76
28.9	Parity configuration.....	77
29.0	Successive approximation analog-to-digital converter (SARADC) .....	80
30.0	Low power comparator (LPCOMP) .....	82
31.0	Watchdog timer (WDT) .....	85
31.1	Reload criteria .....	85
31.2	Temporarily pausing the watchdog.....	85
31.3	Watchdog reset.....	85
32.0	Software Interrupts (SWI) .....	88
33.0	Pulse density modulation interface (PDM) .....	89
33.1	Master clock generator .....	89
33.2	Module operation .....	90
33.3	Decimation filter .....	90
34.0	Digital Voice interface (PCM, I2S) .....	95
34.1	Mode .....	97
34.2	Transmitting and receiving.....	97
34.3	Left right clock (LRCK) .....	98
34.4	Serial clock (SCK) .....	99
34.5	Master clock (MCK) .....	99
34.6	Width, alignment and format .....	100
34.7	Pin configuration .....	102

---

35.0	Pulse Width Modulation (PWM).....	108
35.1	Pin configuration .....	109
35.2	Wave Counter .....	110
35.3	Decoder.....	113
35.4	Limitations.....	120
36.0	Keyboard Scanner .....	121
	Document Revision History.....	122

## 2.0 Introduction

### 2.1 Overview

The SYD8821 chip is highly integrated with ARM® Cortex®-M0 processor, Bluetooth Low Energy v4.2 baseband control core, ROM, Flash, Bluetooth Modem, Radio Transceiver, on-chip Balun and digital interfaces for the BLE application. The Cortex M0 can operate at 64MHz clock rate for heavy thread computing application, and can also operate at lower clock rate for simple data communication purpose. SYD8821 has DCDC converter built-in to provide full-solution SoC for stand-alone applications such as HID and Wearable devices.

错误!未找到引用源。 shows the architecture block diagram of the chip. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

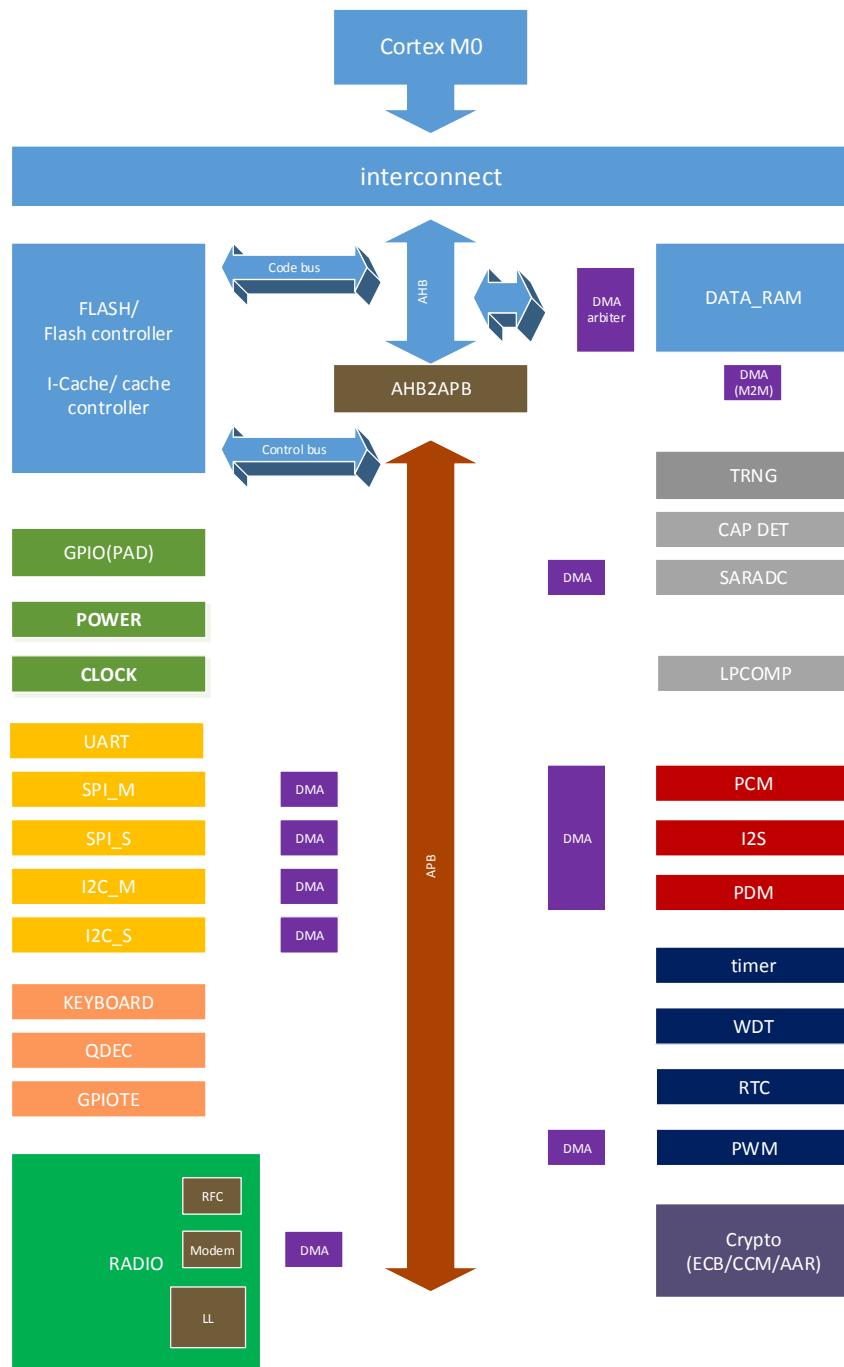


Fig1. SYD8821 Block Diagram

## 3.0 Pin assignments

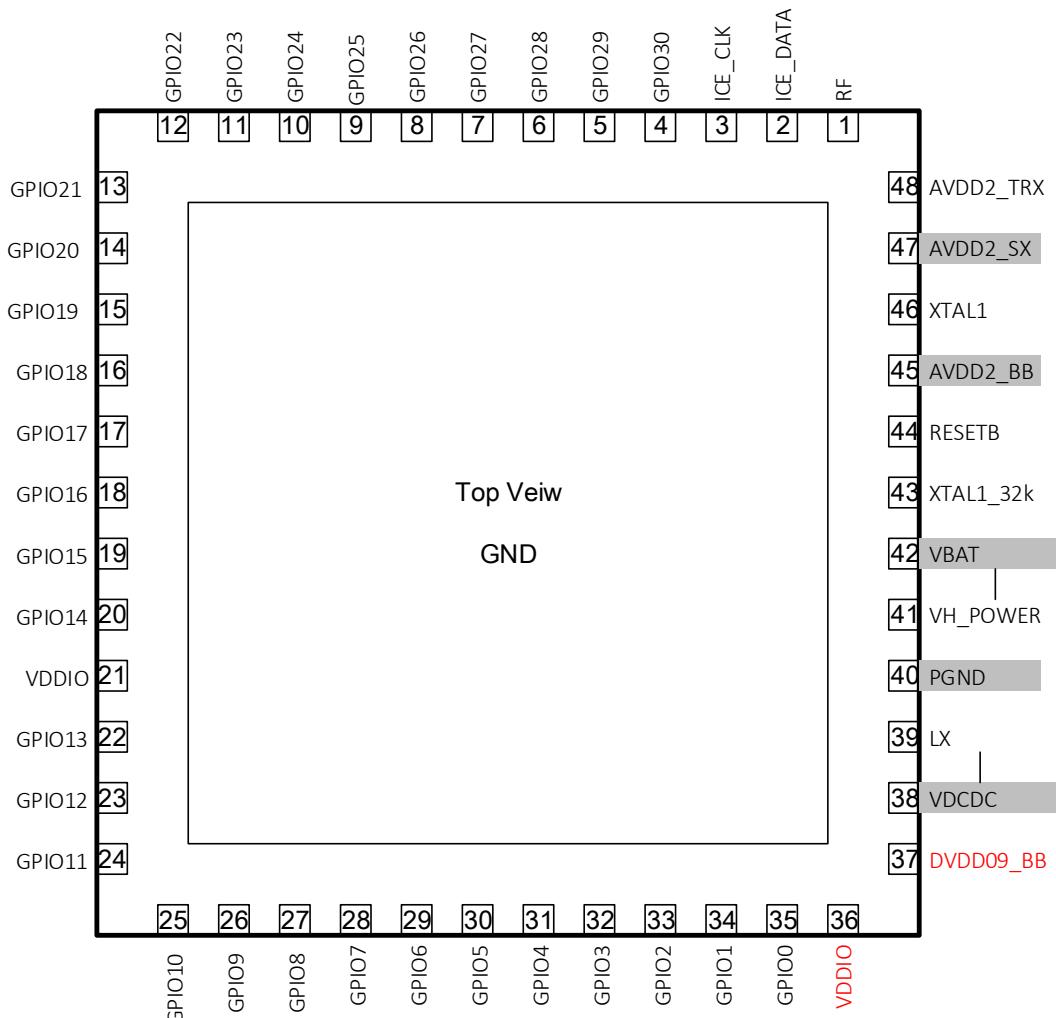


Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
1	RFP	BiDir	2.4GHz transceiver RF port, connected to antenna
2	ICE_DATA	BiDir	Serial debug port interface – DATA GPO, PWM

Pin No.	Signal Name	Type	Description
3	ICE_CLK	BiDir	Serial debug port interface – Clock GPO, PWM
4	GPIO30	BiDir	
5	GPIO29	BiDir	
6	GPIO28	BiDir	
7	GPIO27	BiDir	GPIO, PWM2, or LED2 I <sup>2</sup> C: Data IO, as I2C_SDA0 UART: UART_RXD0
8	GPIO26	BiDir	GPIO, PWM0, or LED0 I <sup>2</sup> C:Clock output, as I2C_SCL0, UART: UART_RXD0
9	GPIO25	BiDir	GPIO, Key_T2, PWM1, or LED1 UART: UART_RTS0
10	GPIO24	BiDir	GPIO, Key_T1, PWM2, or LED2 UART: UART_CTS0
11	GPIO23	BiDir	GPIO, or Key_Z2 I <sup>2</sup> C: Data IO, as I2C_SDA1 UART: UART_RXD1
12	GPIO22	BiDir	GPIO, or Key_Z1 I <sup>2</sup> C:Clock output, I2C_SCL1 UART: UART_RXD1
13	GPIO21	BiDir	GPIO, PWM1, or LED1
14	GPIO20	BiDir	GPIO, PWM2, or LED2 UART: UART_RXD0
15	GPIO19	BiDir	GPIO, PWM0, or LED0 UART: UART_RXD0
16	GPIO18	BiDir	GPIO, PWM1, or LED1 UART: UART_RTS0
17	GPIO17	BiDir	GPIO, PWM2, or LED2 UART: UART_CTS0
18	GPIO16	BiDir	GPIO, MouseKey_B5, PWM0, or LED0 I <sup>2</sup> C:Data IO, I2C_SDA1

Pin No.	Signal Name	Type	Description
19	GPIO15	BiDir	GPIO, MouseKey_B4, PWM1, or LED1 I <sup>2</sup> C:Clock output, I2C_SCL1
20	GPIO14	BiDir	GPIO, MouseKey_CPI, PWM2, or LED2
21	VDDIO	Power	Power for IO, 1.8V~3.6V
22	GPIO13	BiDir	GPIO, MouseKey_Middle
23	GPIO12	BiDir	GPIO, MouseKey_Right
24	GPIO11	BiDir	GPIO, MouseKey_Left
25	GPIO10	BiDir	GPIO Motion_Wake_Up as motion detect for external sensor, active_L
26	GPIO9	BiDir	GPIO SPI4W: Master, Data output, SPI_DO
27	GPIO8	BiDir	GPIO SPI4W:Master, Chip Select, SPI_CSN SPI3W:Master, Chip Select, SPI_CSN
28	GPIO7	BiDir	GPIO SPI4W:Master, Data input, SPI_DI SPI3W:Master, Data IO, SPI_DIO I <sup>2</sup> C:Data IO, I2C_SDA0
29	GPIO6	BiDir	GPIO SPI4W:Master, Clock output, SPI_CLK SPI3W:Master, Clock output, SPI_CLK I <sup>2</sup> C:Clock output, I2C_SCL0
30	GPIO5	BiDir	GPIO SPI4W: Master, Data output, SPI_DO_1 I <sup>2</sup> C:Data IO, I2C_SDA1 UART: UART_TXDO
31	GPIO4	BiDir	GPIO SPI4W: Master, Chip Select, SPI_CSN_1 I <sup>2</sup> C: Clock output, I2C_SCL1 UART: UART_RXDO
32	GPIO3	BiDir	GPIO

Pin No.	Signal Name	Type	Description
			SPI4W:Master, Data input, SPI_DI_1 UART: UART_RTS0
33	GPIO2	BiDir	GPIO, PWM0, or LED0 SPI4W: Master, Clock output, SPI_CLK_1 UART: UART_CTS0
34	GPIO1	BiDir	GPIO, PWM1, or LED1 Analog Input_1 I <sup>2</sup> C:Data IO, I2C_SDA1 UART: UART_TXD1
35	GPIO0	BiDir	GPIO, PWM2, or LED2 Analog Input_0 I <sup>2</sup> C: Clock output, I2C_SCL0 UART: UART_RXDO
36	DVDD15_BB	Power	Internal 1.5V LDO output for baseband, need add 0.1uF capacitor close to Pin33.
37	DVDD18_Flash	Power	Internal 1.8V LDO output for Flash, need add 0.1uF capacitor close to Pin4.
38	VDCDC	Power	Input of internal LDO, and feedback voltage for DCDC.
39	LX	Power	Switch Node with connecting to inductor. Keep pcb trace as short and wide as possible.
40	PGND	Power	GND for DCDC
41	VH_POWER	Power	Boost mode: Output power pin, connected directly to boost output capacitor. Keep pcb trace as short and wide as possible. Buck mode: Input power pin, connector to battery or external power source. Recommend to add de-coupling cap, 10uF. Keep pcb trace as short and wide as possible.
42	VBAT	Power	Provide power for DCDC internal control unit. Keep pcb trace as short and wide as possible.
43	XTAL1_32k	In	Crystal input for 32.768kHz XTAL
44	RESETB	In	Active_L signal for HW reset. Recommended to add RC POR circuit (R=100k, C=100nF) connected to VDDIO power domain.
45	AVDD1_BB	Power	Internal LDO input for baseband analog circuit, need add 0.1uF capacitor close

Pin No.	Signal Name	Type	Description
			to Pin44.
46	XTAL1	In	Crystal input for 16MHz XTAL
47	AVDD1_SX	Power	Internal LDO input for RF_SX circuit, need add 0.1uF capacitor close to Pin47.
48	AVDD1_TRX	Power	Internal LDO input for RF_TRX circuit, need add 0.1uF capacitor close to Pin48.