Preliminary Data Sheet

F1CC8835

IEEE 802.11 a/b/g/n/ac with Bluetooth 4.1 for Automotive

1. General Description

1.1 IEEE 802.11x Features

• IEEE 802.11ac compliant.

• Single-stream spatial multiplexing up to 433.3 Mbps data rate.

• Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).

• Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.

• Supports IEEE 802.11ac/n beamforming.

• Supports standard SDIO v3.0 (including DDR50 mode at 50 MHz and SDR104 mode at 208 MHz, 4-bit and 1-bit), and gSPI (48 MHz) host interfaces.

• Backward compatible with SDIO v2.0 host interfaces.

1.2 Bluetooth Features

• Complies with Bluetooth Core Specification Version 4.1 for automotive applications with provisions for supporting future specifications.

• Bluetooth Class 1 or Class 2 transmitter operation.

• Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.

• Adaptive frequency hopping (AFH) for reducing radio frequency interference.

• Interface support, host controller interface (HCI) using a high-speed UART interface and PCM for audio data.

• Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.

• Automatic frequency detection for standard crystal and TCXO values.

• Supports low energy host wake-up for long term system sleep capability.

1.3 General Features

• Supports battery voltage range from 3.0V to 4.8V supplies with internal switching regulator.

• Programmable dynamic power management

• OTP: 502 bytes of user-accessible memory

• Package: 48 pin LGA (14.2 mm x 12.6 mm x 2.5mm)

• Security:

  – WPA™ and WPA2™ (Personal) support for powerful encryption and authentication

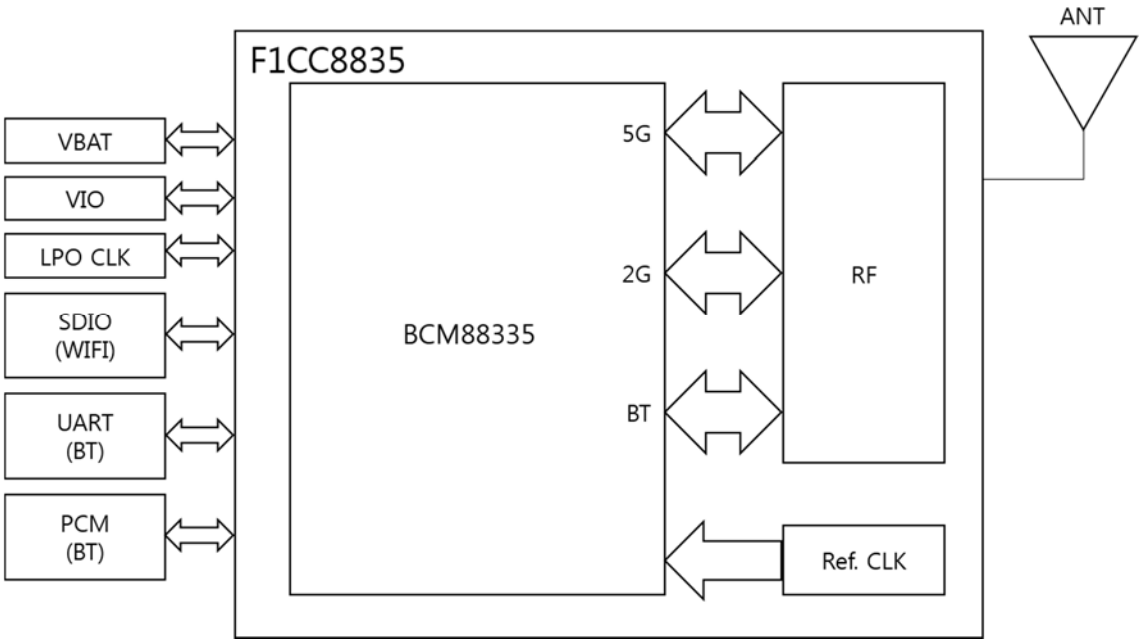
  – AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility

  – Reference WLAN subsystem provides Cisco® Compatible Extensions (CCX, CCX 2.0, CCX 3.0, CCX 4.0, CCX 5.0)

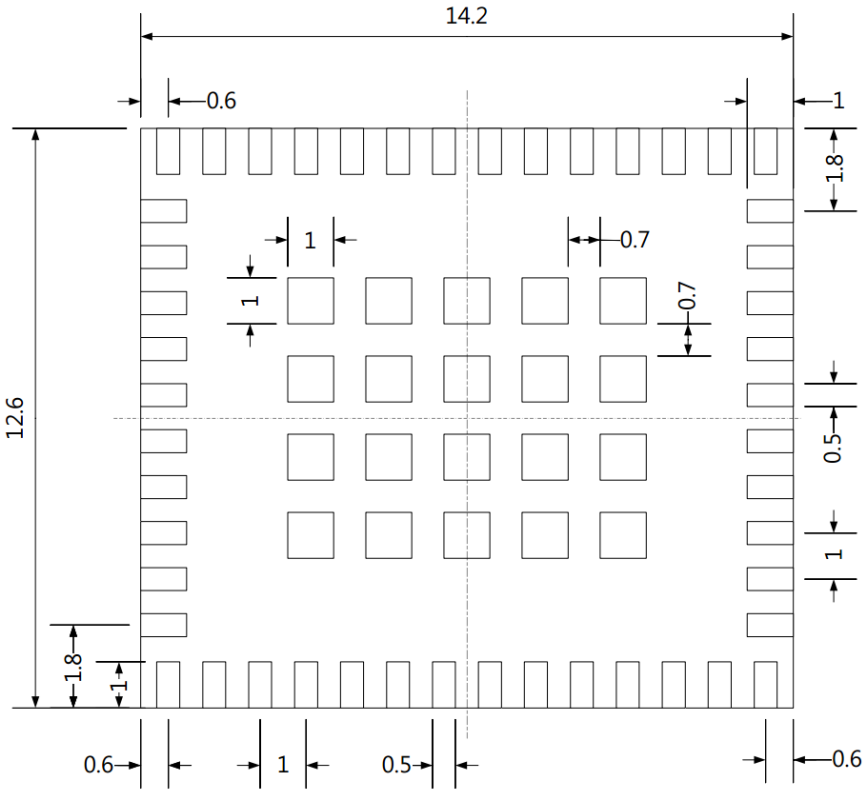
  – Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)

• Worldwide regulatory support: Global products supported with worldwide homologated design.

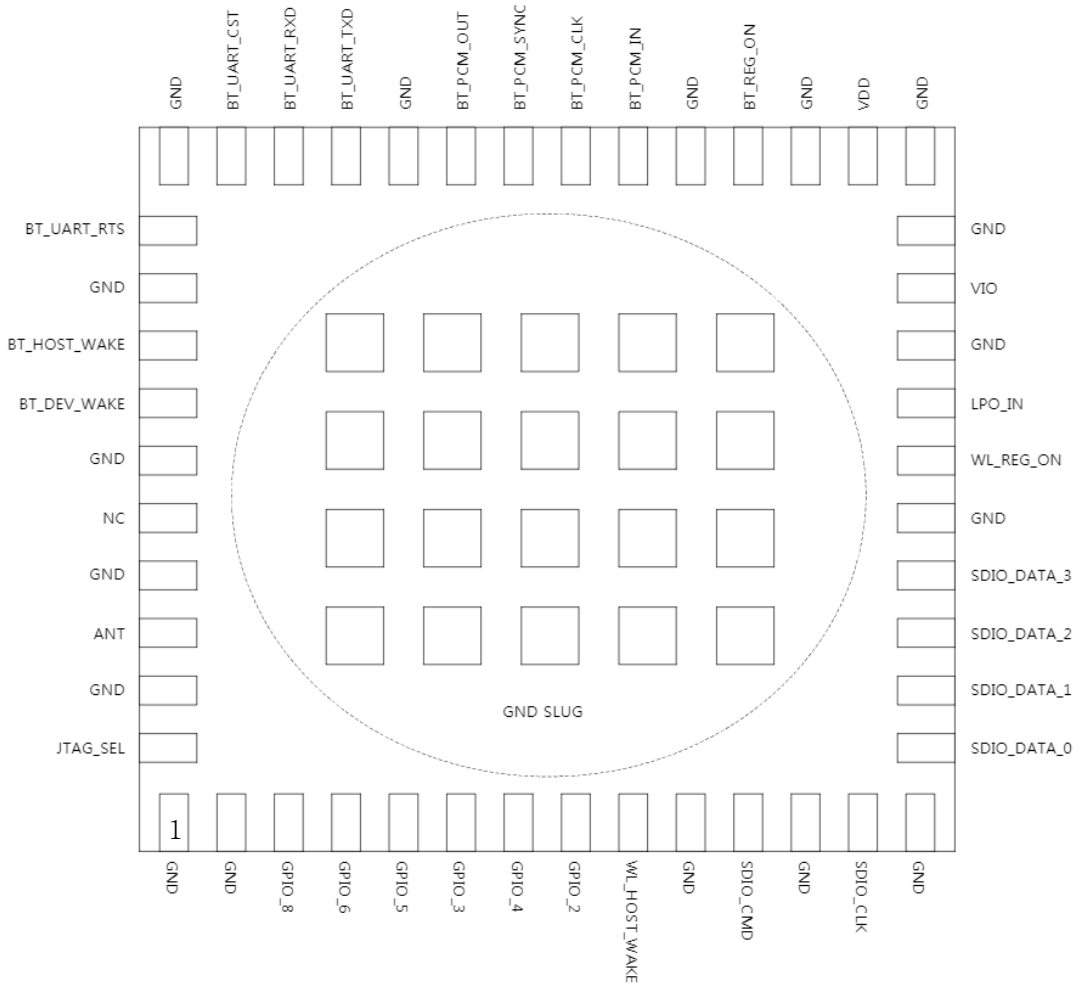
2. Block Diagram



3. Package Dimensions



4. Pin Layout



< Top View>

PinNo	Description	PinNo	Description	PinNo	Description
1	GND	24	GND	47	GND
2	GND	25	GND	48	JTAG_SEL
3	GPIO_8	26	VDD	49	GND
4	GPIO_6	27	GND	50	GND
5	GPIO_5	28	BT_REG_ON	51	GND
6	GPIO_3	29	GND	52	GND
7	GPIO_4	30	BT_PCM_IN	53	GND
8	GPIO_2	31	BT_PCM_CLK	54	GND
9	WL_HOST_WAKE	32	BT_PCM_SYNC	55	GND
10	GND	33	BT_PCM_OUT	56	GND
11	SDIO_CMD	34	GND	57	GND

12	GND	35	BT_UART_TXD	58	GND
13	SDIO_CLK	36	BT_UART_RXD	59	GND
14	GND	37	BT_UART_CTS	60	GND
15	SDIO_DATA_0	38	GND	61	GND
16	SDIO_DATA_1	39	BT_UART_RTS	62	GND
17	SDIO_DATA_2	40	GND	63	GND
18	SDIO_DATA_3	41	BT_HOST_WAKE	64	GND
19	GND	42	BT_DEV_WAKE	65	GND
20	WL_REG_ON	43	GND	66	GND
21	LPO_IN	44	NC	67	GND
22	GND	45	GND	68	GND
23	VIO	46	ANT		

5. Terminal Functions and Descriptions

5.1 WLAN SDIO Bus Interface

Pin No.	Signal Name	Description	Type
13	SDIO_CLK	SDIO clock input.	I
11	SDIO_CMD	SDIO command line.	I/O
15	SDIO_DATA_0	SDIO data line 0.	I/O
16	SDIO_DATA_1	SDIO data line 1.	I/O
17	SDIO_DATA_2	SDIO data line 2.	I/O
18	SDIO_DATA_3	SDIO data line 3.	I/O

5.2 WLAN GPIO Interface

Pin No.	Signal Name	Description	Type
9	WL_HOST_WAKE /GPIO 0	Programmable GPIO pins.	I/O
8	GPIO_2	Programmable GPIO pins.	I/O
6	GPIO_3	Programmable GPIO pins.	I/O
7	GPIO_4	Programmable GPIO pins.	I/O
5	GPIO_5	Programmable GPIO pins.	I/O
4	GPIO_6	Programmable GPIO pins.	I/O
3	GPIO_8	Programmable GPIO pins.	I/O

5.3 JTAG Interface

Pin No.	Signal Name	Description	Type
48	JTAG_SEL	JTAG select. Pull high to select the JTAG interface. If the JTAG interface is not used, this pin may be left floating or connected to ground.	I/O

5.4 Clocks

Pin No.	Signal Name	Description	Type
21	LPO_IN	External sleep clock input(32.768 kHz).	I

5.5 Bluetooth PCM

Pin No.	Signal Name	Description	Type
31	BT_PCM_CLK	PCM clock; can be master(output) or slave (input).	I/O
30	BT_PCM_IN	PCM data input.	I
33	BT_PCM_OUT	PCM data output.	O
32	BT_PCM_SYNC	PCM sync; can be master(output) or slave (input).	I/O

5.6 Bluetooth UART

Pin No.	Signal Name	Description	Type
37	BT_UART_CTS	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	I
39	BT_UART_RTS	UART request-to-send. Activelow request-to-send signal for the HCI UART interface.	O
36	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.	I
35	BT_UART_TXD	UART serial output. Serial data output for the HCI UART interface.	O

5.7 Miscellaneous

Pin No.	Signal Name	Description	Type
20	WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pulldown resistor that is enabled by default. It can be disabled through programming.	I
28	BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.	I
42	BT_DEV_WAKE	Bluetooth DEV_WAKE.	I/O

41	BT_HOST_WAKE	Bluetooth HOST_WAKE.	I/O
44	NC	No connect	

5.8 Voltage Supplies

Pin No.	Signal Name	Description	Type
26	VDD	Power VBAT.	I
23	VIO	1.8V–3.3V supply for pads	I
1, 2, 10, 12,14,19,22, 24,25,27,29, 34,38,40,43, 45,47,	GND	Power Ground	
49-68	GND	Ground slug	

5.9 RF Interface

Pin No.	Signal Name	Description	Type
46	ANT	2.4 GHz and 5 GHz RF	I/O

6. WLAN GPIO Signals and Strapping Options

6.1 WLAN GPIO Functions and Strapping Options

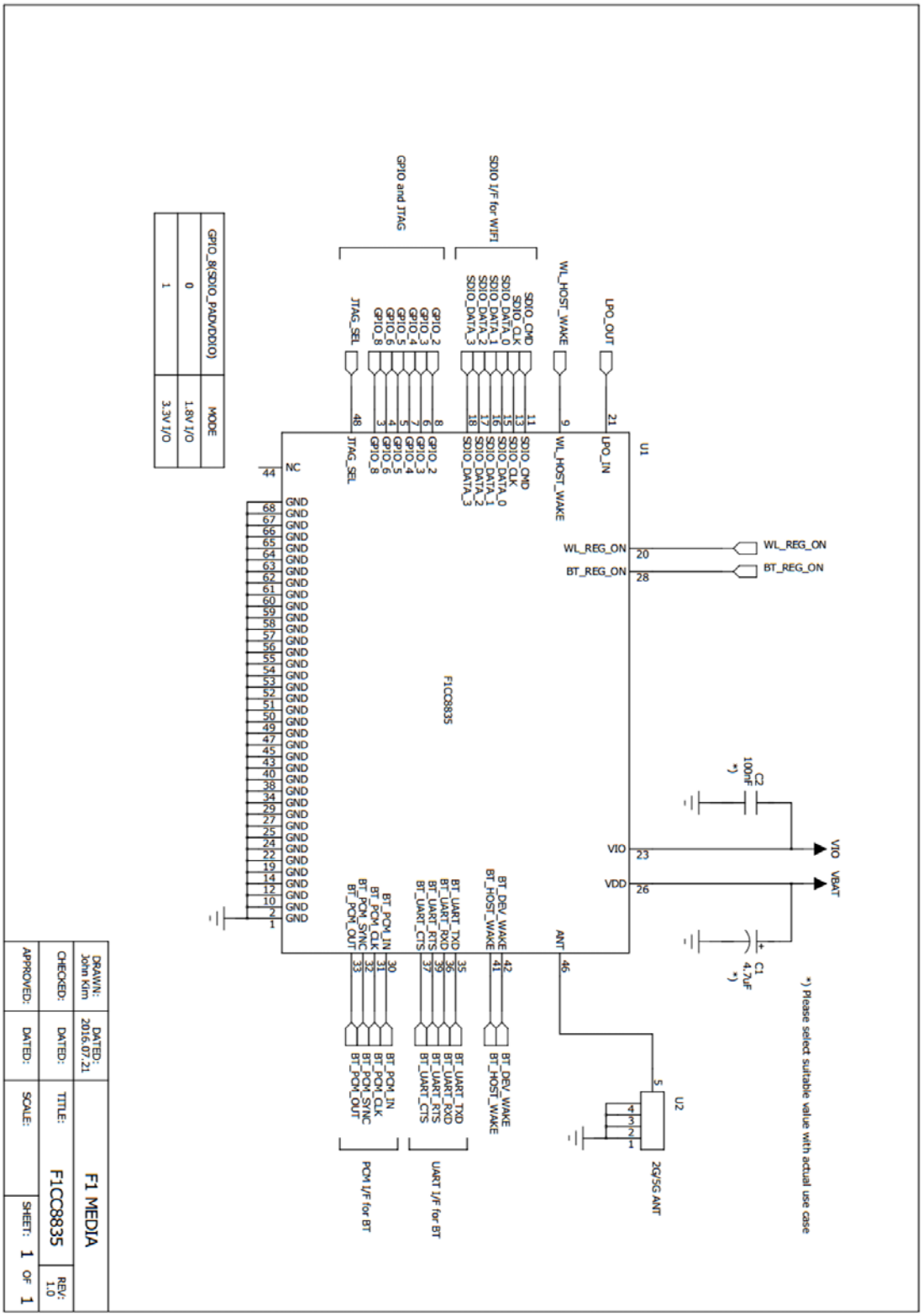
Strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less. SDIO v3.0 is only applicable at VIO=1.8V.

Pin No.	Pin Name	Description	Default Function
3	GPIO_8	SDIO_PADVDDIO	0

6.2 SDIO I/O Voltage Selection

SDIO_PADVDDIO.	Mode
0	1.8V I/O
1	3.3V I/O

7. Reference Schematic Circuit



8. Power Management

VDD and VIO can be provided by the regulators inside F1CC8835 module.
Two control signals, BT_REG_ON and WL_REG_ON are used to power-up the regulators and take the respective section out of reset.
All regulators are powered down only when both BT_REG_ON and WL_REG_ON are deasserted.

8.1 WLAN Power Management

F1CC8835 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the F1CC8835 into various power management states. The power management unit enables and disables internal regulators. Power up sequences are fully programmable. Free running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used whenever possible.

The F1CC8835 WLAN power states are described as follows:
• Active mode – All WLAN blocks are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and clock speeds are dynamically adjusted by the PMU sequencer.
• Doze mode – The radio, analog domains and most of the linear regulators are powered down. All main clocks (PLL, crystal oscillator) are shut down. The 32.768kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode.
• Deep-sleep mode – Most of the chip including both analog and digital domains and most of the regulators are powered off. Logic states in the digital core are saved and preserved into a retention memory in the always-ON domain. Upon a wake-up event triggered by the PMU timers, an external interrupt or a host resume through the SDIO bus.
• Power-down mode – The F1CC8835 is effectively powered off by shutting down all internal regulators.

8.2 Power-Off Shutdown

The F1CC8835 provides low-power shutdown feature that allows the device to be turned off while the host and any other devices in the system, remain operational. This allows the BWR-8910 to be effectively off while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.
During a low-power shut-down state, all outputs are tri-stated, and most inputs signals are disabled.
When the F1CC8835 is powered on from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

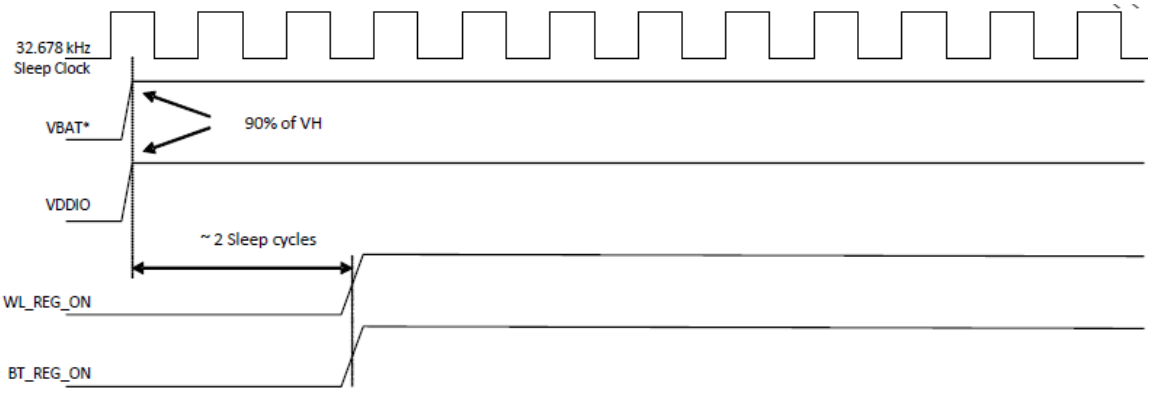
8.3 Power-Up/Power-Down/Reset Circuits

The F1CC8835 has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences.

Signal	*Description*
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal regulators. - HIGH, the regulators are enabled and the WLAN section is out of reset. - LOW, the WLAN section is in reset. - BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. This pin has an internal 200kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

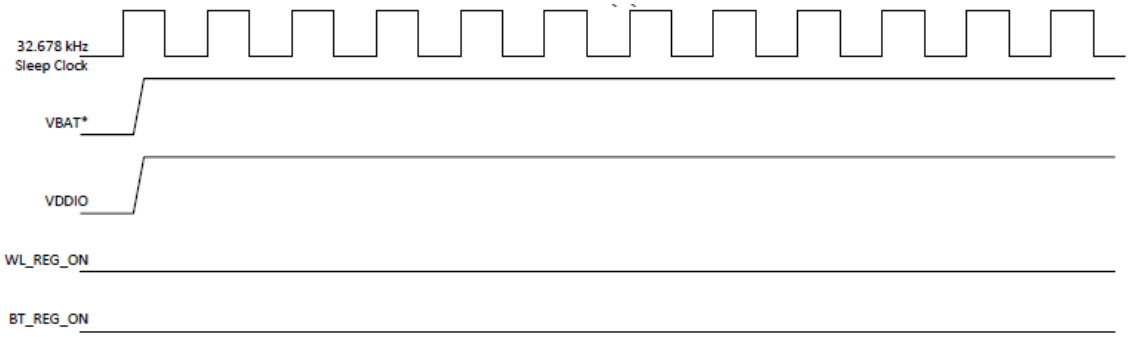
8.4 Power-Up Sequence and Timing

1. WLAN = ON, Bluetooth = ON



*Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

2. WLAN = OFF, Bluetooth = OFF



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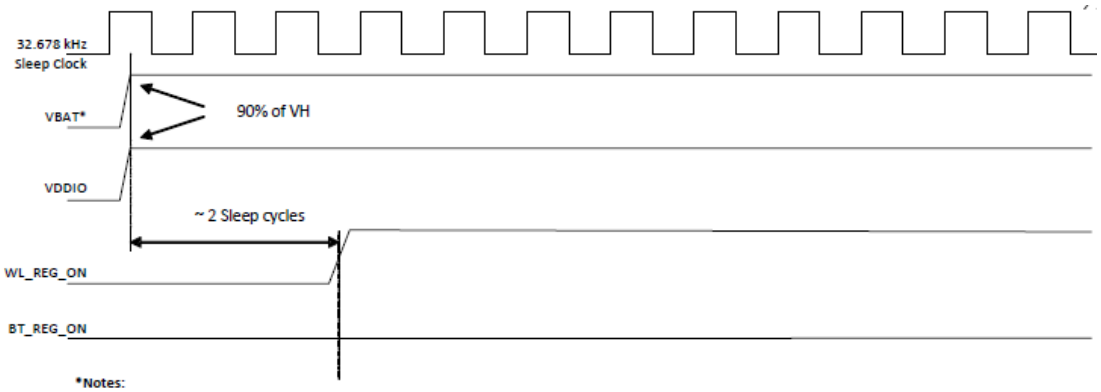
3. WLAN = ON, Bluetooth = OFF



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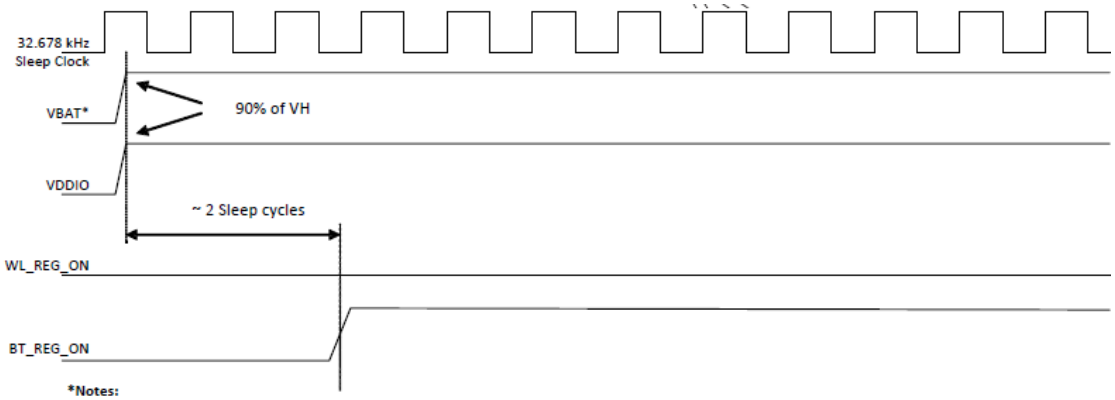
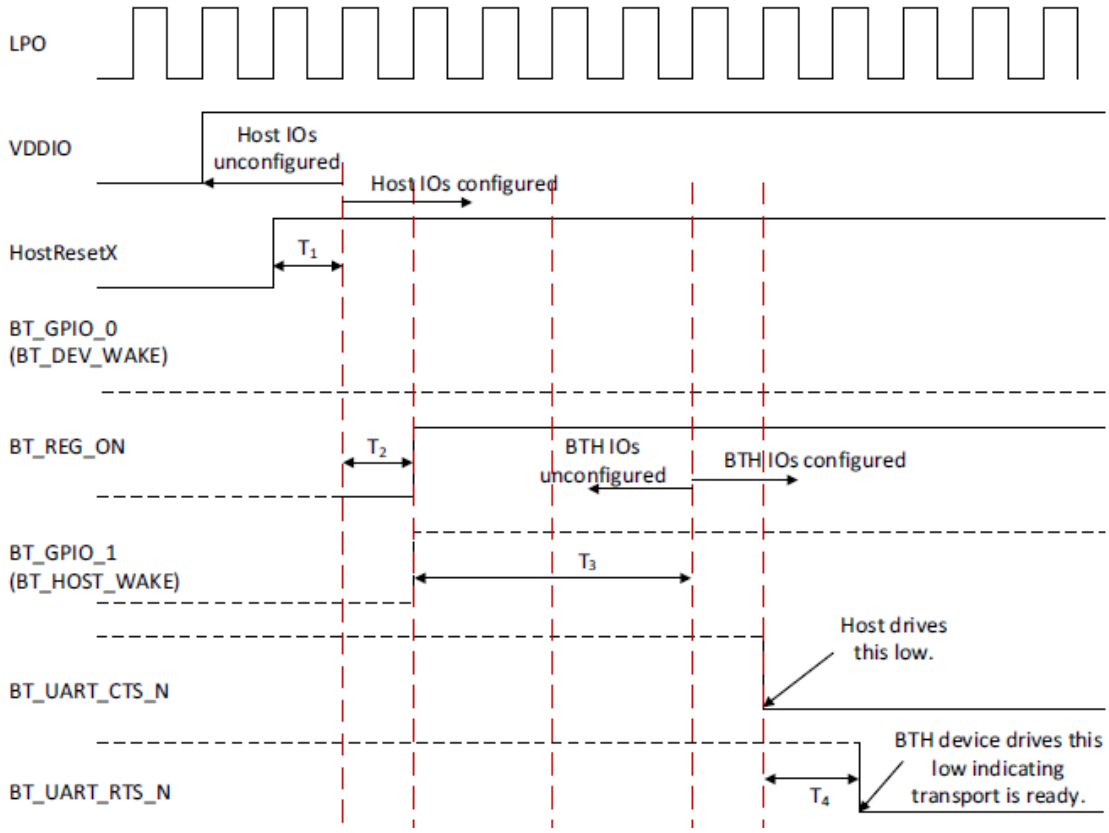
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

4. WLAN = OFF, Bluetooth = ON



*Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds or slower than 10 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

5. Startup Signaling Sequence



- T_1 is the time for the host to settle its IOs after a reset.
- T_2 is the time for the host to drive BT_REG_ON high after the host IOs are configured.
- T_3 is the time for the BTH device to settle its IOs after a reset and the reference clock settling time has elapsed.
- T_4 is the time for the BTH device to drive BT_UART_RTS_N low after the host drives BT_UART_CTS_N low. This assumes the BTH device has completed initialization.

9. Hardware Interfaces

9.1 UART Interface – Bluetooth Host Interfaces

F1CC8835 has a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-bytes receive FIFO and a 1040-bytes transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB(in BCM4335) interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4, a custom Extended H4 and H5. The default baud rate is 115.2Kbaud.

The UART supports the 3-wire H5 UART transport as described in the Bluetooth specification ("Three-wire UART Transport Layer"). Compared to H4, the H5 UART transport reduce the number of signal lines required by eliminating the CTS and RTS signals.

The F1CC8835 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

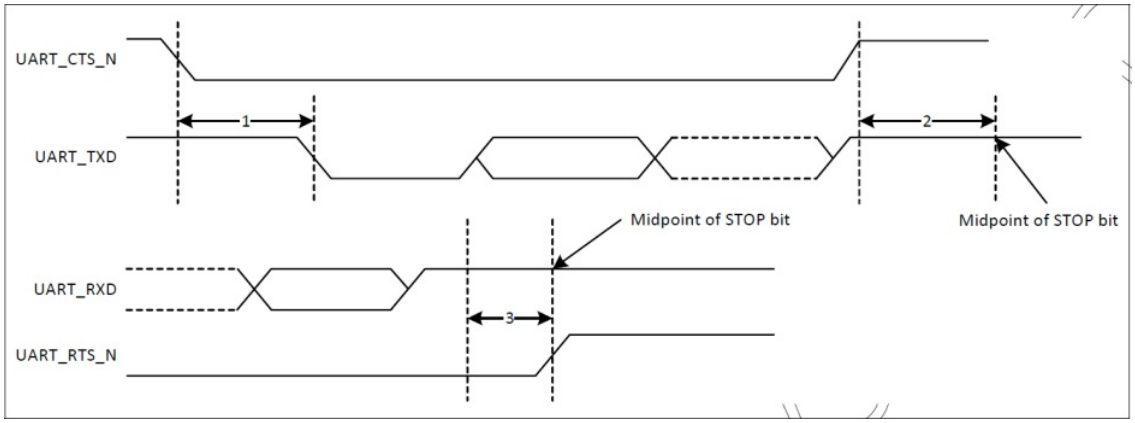
Normally, the UART baud rate is set by a configuration record downloaded after device reset or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The F1CC8835 UART operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

<Example of Common Baud Rates>

Desired Rate	*Actual Rate*	*Error (%)*
4,000,000	4,000,000	0.00
3,692,000	3,692,308	0.01
3,000,000	3,000,000	0.00
2,000,000	2,000,000	0.00
1,500,000	1,500,000	0.00
1,444,444	1,454,544	0.70
921,600	923,077	0.16
460,800	461,538	0.16
230,400	230,796	0.17
115,200	115,385	0.16
57,600	57,692	0.16
38,400	38,400	0.00
28,800	28,846	0.16

19,200	19,200	0.00
14,400	14,423	0.16
9,600	9,600	0.00

<UART Timing>



Ref No.	*Characteristics*	*Min*	*Typ*	*Max*	*Unit*
1	Delay time, UART_CTS_N low to UART_TXD valid	-	-	1.5	Bit period
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit period
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	-	0.5	Bit period

9.2 SDIO WLAN Host Interfaces

F1CC8835 WLAN section provide support for SDIO version 3.0, including the new UHS-I mode:

DS: Default speed(DS) up to 25MHz, including 1-and 4-bit modes (3.3V signaling).

HS: High speed(HS) up to 50MHz (3.3V signaling).

SDR12: SDR up to 25MHz (1.8V signaling).

SDR25: SDR up to 50MHz (1.8V signaling).

SDR50: SDR up to 100MHz (1.8V signaling).

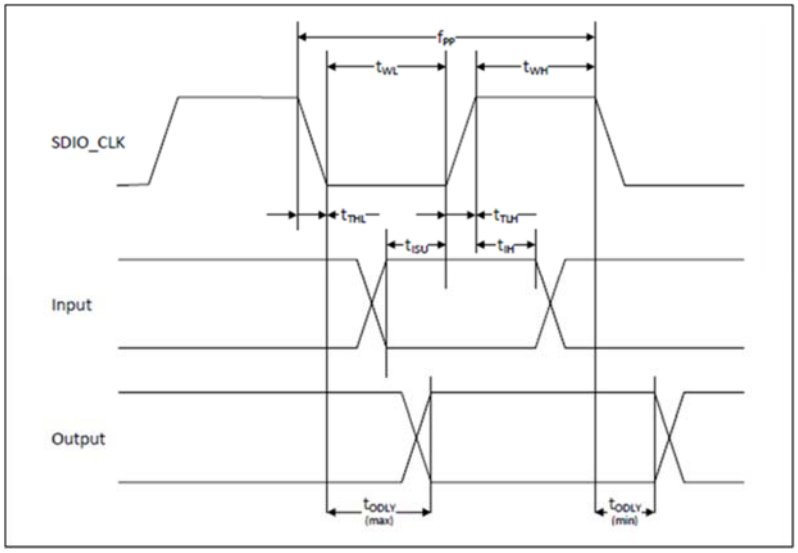
SDR104: SDR up to 208MHz (1.8V signaling).

DDR50: DDR up to 50MHz (1.8V signaling).

- Note: The F1CC8835 is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

9.2.1 SDIO Default Mode Timing

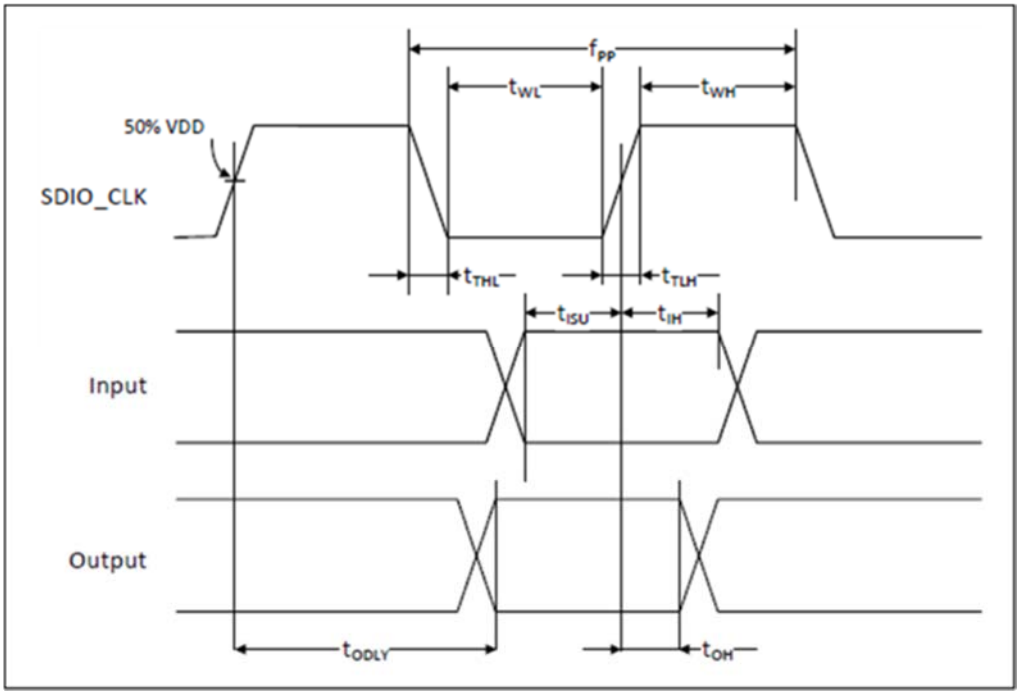


SDIO Bus Timing[a] Parameters (Default Mode)	*Symbol*	*Value*			
		Min.	*Typ.*	*Max.*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	-	25	MHz
Frequency – Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data

b. Min.(Vih) = 0.7xVIO_SDIO and max.(Vil) = 0.2xVIO_SDIO.

9.2.2 SDIO High-Speed Mode Timing



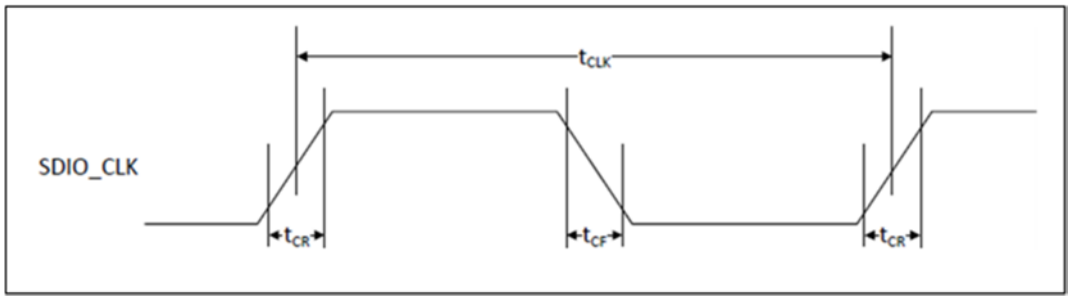
SDIO Bus Timing[a] Parameters (High-Speed Mode)	*Symbol*	*Value*			
		Min.	*Typ.*	*Max.*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	-	25	MHz
Frequency – Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data

b. Min.(Vih) = 0.7xVIO_SDIO and max.(Vil) = 0.2xVIO_SDIO.

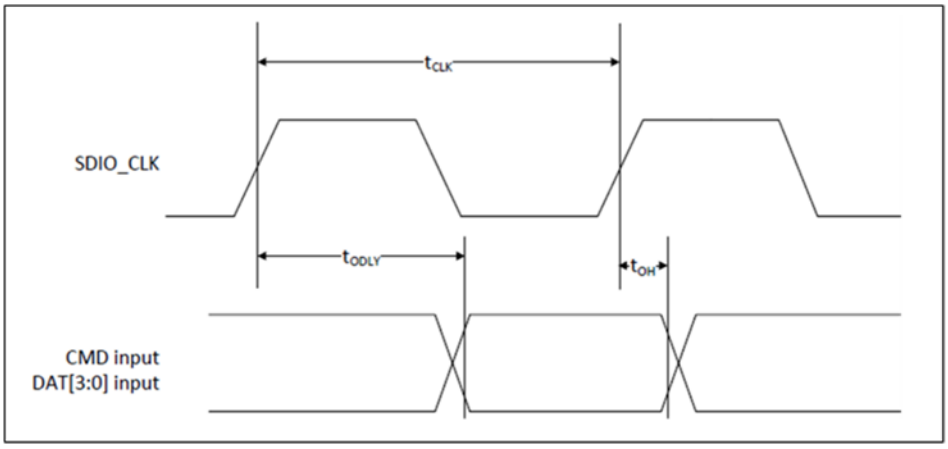
9.2.3 SDIO Bus Timing Specification in SDR Modes

9.2.3.1 Clock Timing



Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Comments*
-	t_{CLK}	40	-	ns	SDR12 mode
		20	-	ns	SDR25 mode
		10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 mode
	t_{CR}, t_{CF}	-	0.2 x t_{CLK}	ns	t_{CR}, t_{CF} < 2.00ns (max) @ 100MHz, C_{CARD} = 10pF) t_{CR}, t_{CF} < 0.96ns (max) @ 208MHz, C_{CARD} = 10pF)
Clock duty cycle	-	30	70	%	-

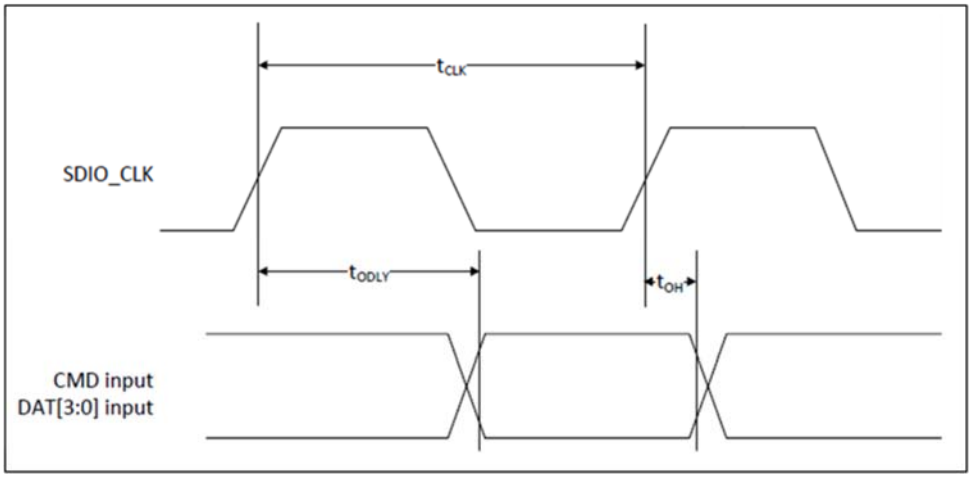
9.2.3.1 Device Input Timing



Symbol	*Min.*	*Max.*	*Unit*	*Comments*
SDR104 Mode				

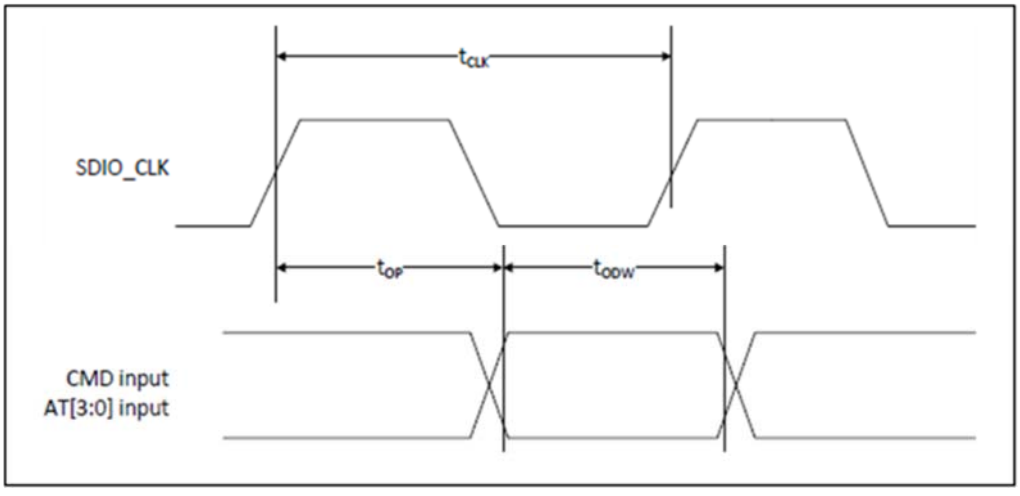
t_{IS}	1.4	-	ns	C_{CARD} = 10pF, VCT = 0.975V
t_{IH}	0.8	-	ns	C_{CARD} = 5pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.0	-	ns	C_{CARD} = 10pF, VCT = 0.975V
t_{IH}	30	70	%	C_{CARD} = 5pF, VCT = 0.975V

9.2.3.2 Device Input Timing (SDR Modes up to 100MHz)



Symbol	*Min.*	*Max.*	*Unit*	*Comments*
t_{ODLY}	-	7.5	ns	t_{CLK} ≥ 10ns C_L = 30pF using driver type B for SDR50
t_{ODLY}	-	14.0	ns	t_{CLK} ≥ 20ns C_L = 40pF using driver SDR12, SDR25
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min) C_L = 15pF

9.2.3.2 Device Input Timing (SDR Modes up to 100MHz to 208 MHz)

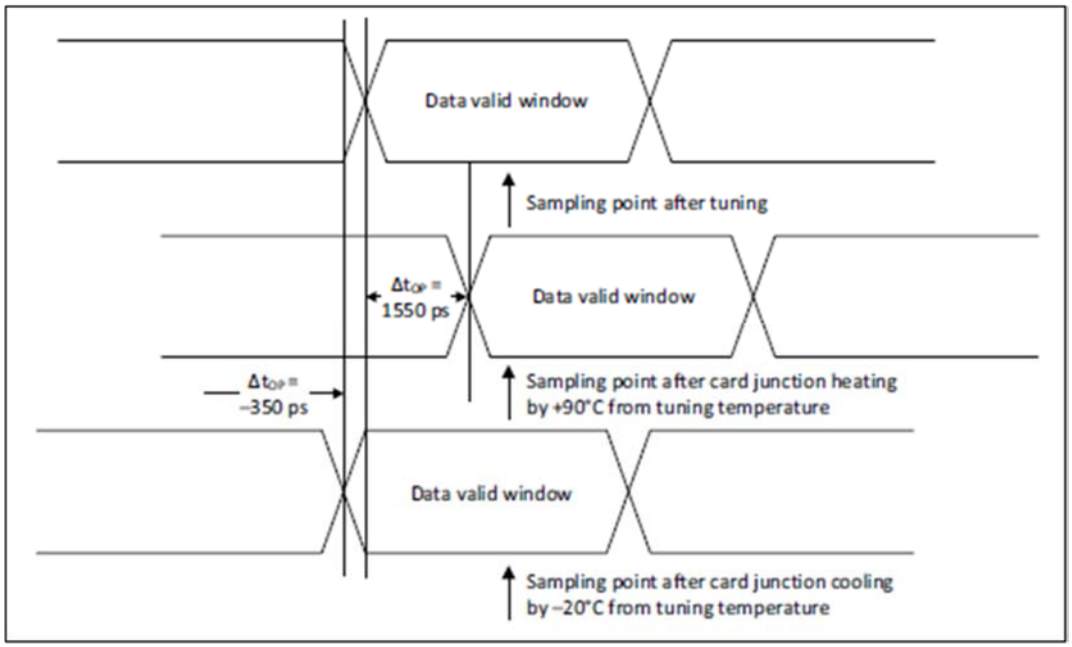


Symbol	*Min.*	*Max.*	*Unit*	*Comments*
t_{OP}	-	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns @208 MHz

Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation

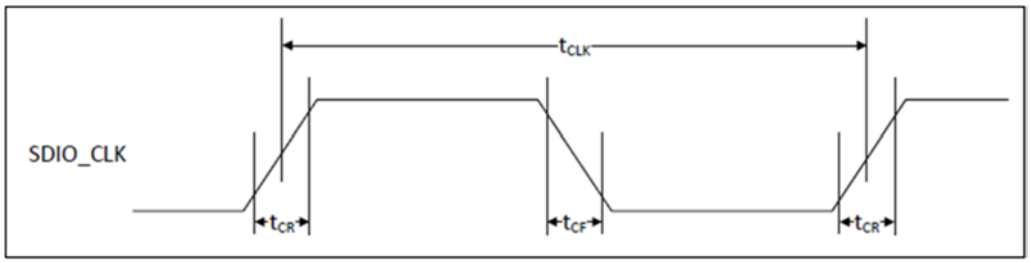
Δt_{OP} = -350 ps for junction temperature of Δt_{OP} = -20 degrees during operation

Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = -20 to +125 degrees during operation



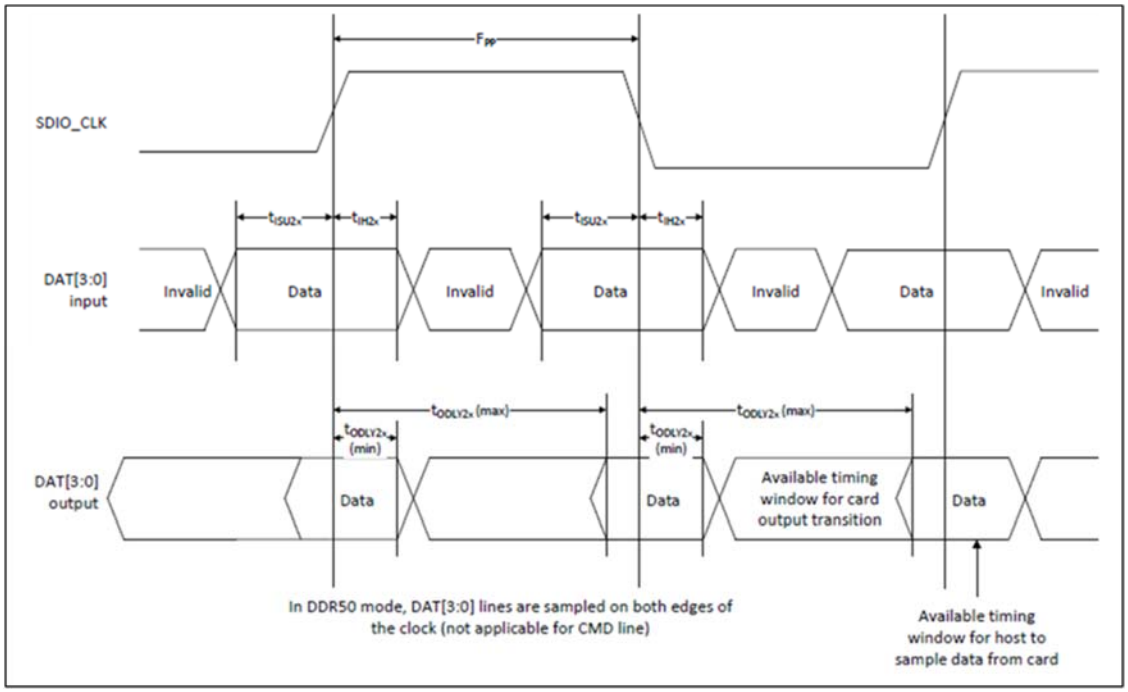
[Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)]

9.2.4 SDIO Bus Timing Specification in DDR50 Mode



Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Comments*
-	t_{CLK}	20	-	ns	DDR50 mode
-	t_{CR}, t_{CF}	-	0.2 x t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max) @ 100MHz, C_{CARD} = 10pF)
Clock duty cycle	-	45	55	%	-

9.2.4.1 Data Timing, DDR50 Mode



Parameter	*Symbol*	*Min.*	*Max.*	*Unit*	*Comments*
Input CMD					
Input setup time	t_{ISU}	6	-	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} < 10pF (1 Card)

Output CMD					
Output delay time	t_{ODLY}	-	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	t_{OH}	1.5	-	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	-	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{CARD} < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	-	7.5	ns	C_{CARD} < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	-	ns	C_{CARD} < 15pF (1 Card)

9.3 PCM Interfaces

F1CC8835 support a PCM interface that can connect to linear PCM Codec devices in master or slave mode. In master mode, the F1CC8835 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the F1CC8835.
The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

9.3.1 Slot Mapping

The F1CC8835 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8 and 16 respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tri-states its output on unused slots to allow other devices to share the PCM interface signals. The data output driver tri-states its output after the falling edge of the PCM clock during the last bit of the slot.

9.3.2 Frame Synchronization

The F1CC8835 supports both short- and long-frame synchronization in both master and slave modes. in short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

9.3.3 Data Formatting

The F1CC8835 may be configured to generate and accept several different data formats. For conventional narrowband speech, the F1CC8835 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM frame. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit or a programmed value on the output. The default format is 1-bit 2's complement data, left justified and clocked MSB first.

9.3.4 Wideband Speech Support

When the host encodes Wideband Speech (WBS) packets in transparent mode. the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate, The F1CC8835 also supports slave transparent mode using a proprietary rate-matching scheme. In SBC-code mode, Linear 16-bit data at 16 kHz (256 Kbps rate) is

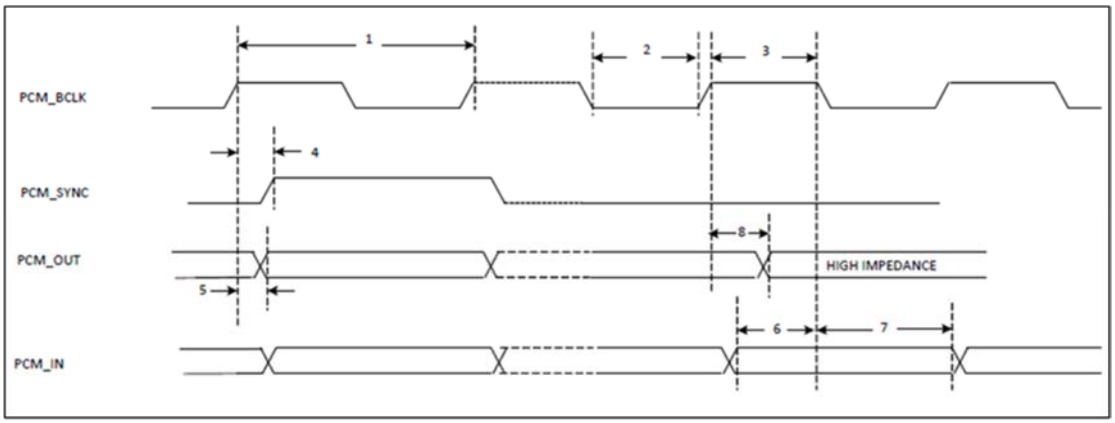
transferred over the PCM bus.

9.3.5 Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24MHz. This mode of operation is initiated with an HCI command from the host.

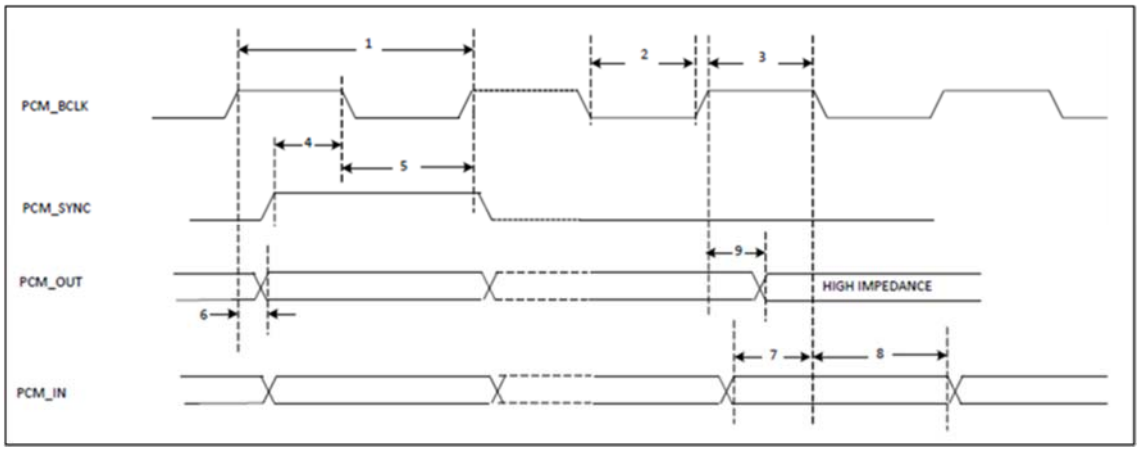
9.3.6 PCM Interface Timing

9.3.6.1 Short Frame Sync, Master Mode



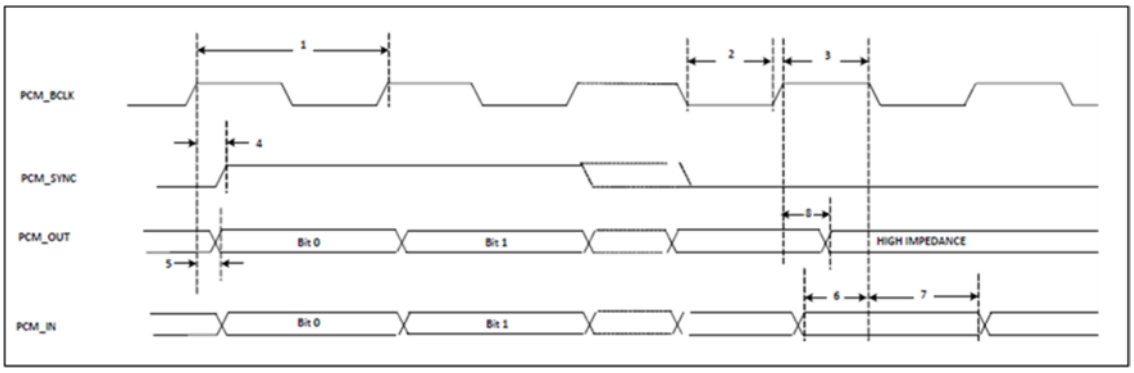
Ref No.	*Characteristics*	*Min.*	*Typ.*	*Max.*	*Unit*
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	-	-	25	ns

9.3.6.2 Short Frame Sync, Slave Mode



Ref No.	*Characteristics*	*Min.*	*Typ.*	*Max.*	*Unit*
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

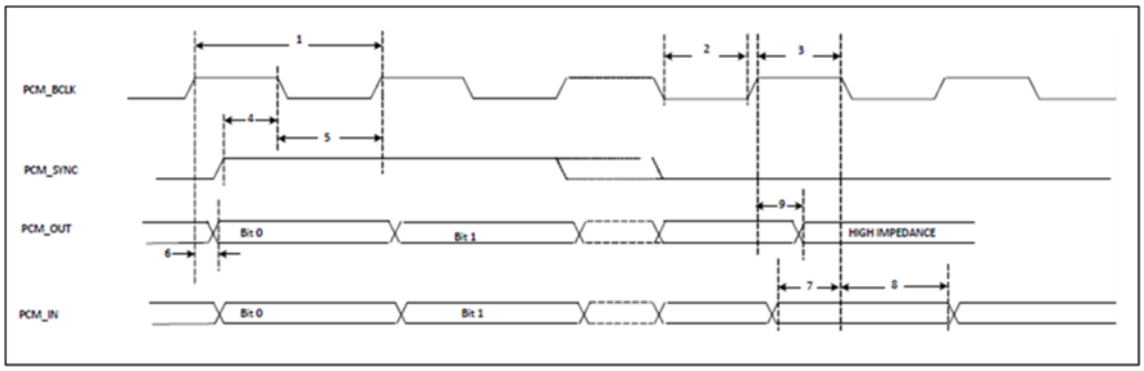
9.3.6.3 Long Frame Sync, Master Mode



Ref No.	*Characteristics*	*Min.*	*Typ.*	*Max.*	*Unit*
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns

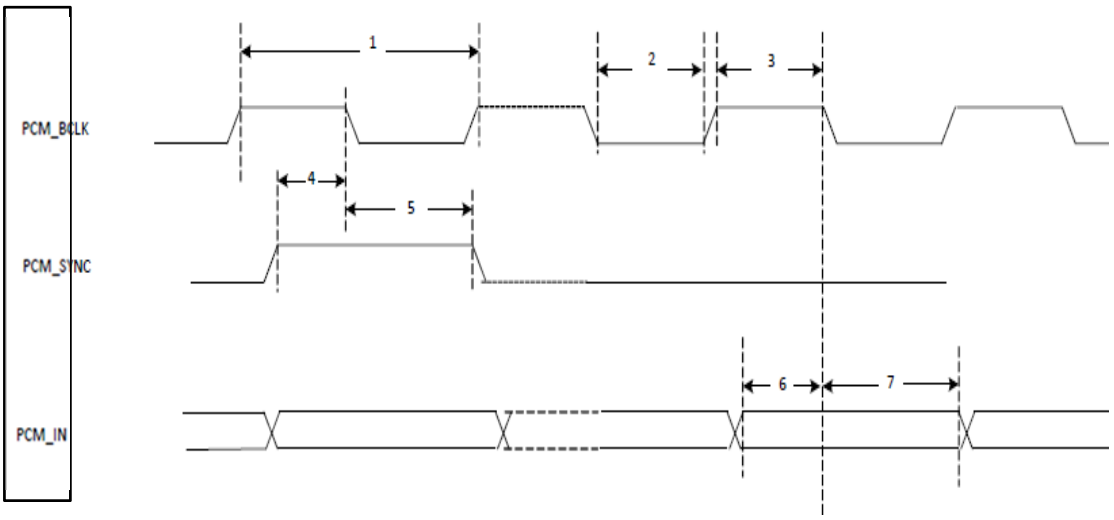
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

9.3.6.4 Long Frame Sync, Slave Mode



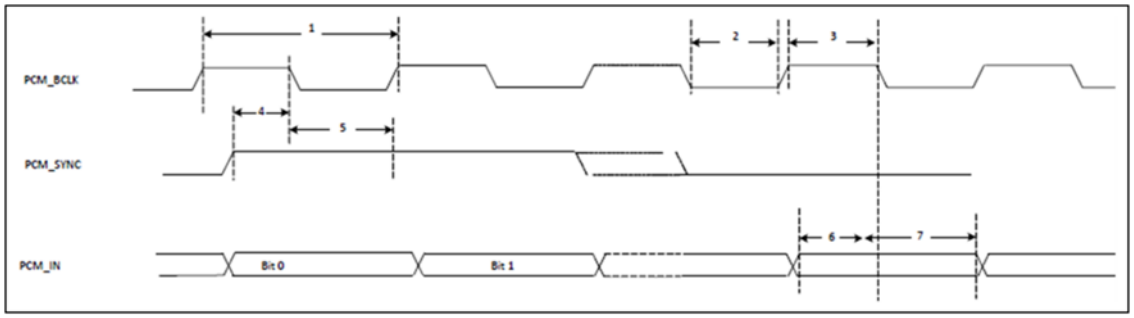
Ref No.	*Characteristics*	*Min.*	*Typ.*	*Max.*	*Unit*
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

9.3.6.5 Short Frame Sync, Burst Mode



Ref No.	*Characteristics*	*Min.*	*Typ.*	*Max.*	*Unit*
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

9.3.6.6 Long Frame Sync, Burst Mode



Ref No.	*Characteristics*	*Min.*	*Typ.*	*Max.*	*Unit*
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns

5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

10. Electronical Characteristics

10.1 Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
DC Supply Voltage	VDD (a)	-0.5	+6	V
	VIO	-0.5	+3.9	V
Maximum undershoot voltage for I/O (b)	Vundershoot	-0.5	-	V
Maximum overshoot voltage for I/O (b)	Vovershoot	-	VIO+0.5	V
Maximum junction temperature	Tj	-	125	Deg. C

(a). The maximum continuous voltage is 4.8V. Voltage transients up to 6.0V (for up to 10 seconds), cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.0V (for up to 250 seconds), cumulative duration over the lifetime of the device, are allowed.

(b). Duration not to exceed 25% of the duty cycle.

10.2 Environmental Ratings

Characteristic	Minimum	Maximum	Unit	Conditions/Comments
Ambient Temperature	-40	+85	Deg. C	Functional operation
Storage Temperature	-40	+125	Deg. C	
Relative Humidity	-	60	%	Storage
	-	85	%	Operation

10.3 Recommended Operating Conditions and DC Characteristics

Parameter		Minimum	Typical	Maximum	Unit
DC supply voltage	VDD	3.0(a)	-	4.8(b)	V
	VIO	1.71	-	3.63	V
SDIO Interface I/O Pins					
For VIO_SDIO = 1.8V					
Input high voltage	VIH	1.27	-	-	V
Input low voltage	VIL	-	-	0.58	V
Output high voltage @ 2 mA	VOH	1.40	-	-	V
Output low voltage @ 2 mA	VOL	-	-	0.45	V
For VIO_SDIO = 3.3V					
Input high voltage	VIH	0.625 x VIO	-	-	V
Input low voltage	VIL	-	-	0.25 x VIO	V
Output high voltage @ 2 mA	VOH	0.75 x VIO	-	-	V

Output low voltage @ 2 mA	VOL	-	-	0.125 x VIO	V
Other Digital I/O Pins = 1.8 V					
Input high voltage	VIH	0.65 x VIO	-	-	V
Input low voltage	VIL	-	-	0.35 x VIO	V
Output high voltage @ 2 mA	VOH	VIO - 0.45	-	-	V
Output low voltage @ 2 mA	VOL	-	-	0.45	V
Other Digital I/O Pins = 3.3V					
Input high voltage	VIH	2.00	-	-	V
Input low voltage	VIL	-	-	0.80	V
Output high voltage @ 2 mA	VOH	VIO - 0.4	-	-	V
Output low voltage @ 2 mA	VOL	-	-	0.40	V

a. The BCM88335 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.13V < VBAT < 4.8V.

b. The maximum continuous voltage is 4.8V. Voltage transients up to 6.0V (for up to 10 seconds), cumulative duration over the lifetime of the device are allowed. Voltage transients as high as 5.0V (for up to 250 seconds), cumulative duration over the lifetime of the device are allowed.

10.4 DC/RF Characteristics

10.4.1 WLAN 5 GHz Receiver Characteristics

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	-	4900	-	5845	MHz
RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)	6 Mbps OFDM	-	-94.5	-	dBm
	9 Mbps OFDM	-	-93.1	-	dBm
	12 Mbps OFDM	-	-92.2	-	dBm
	18 Mbps OFDM	-	-89.6	-	dBm
	24 Mbps OFDM	-	-86.3	-	dBm
	36 Mbps OFDM	-	-83	-	dBm
	48 Mbps OFDM	-	-78.3	-	dBm
	54 Mbps OFDM	-	-76.8	-	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) Defined for default parameters : 800 ns	20 MHz channel spacing for all MCS rates				
	MCS0	-	-94	-	dBm
	MCS1	-	-91.7	-	dBm
	MCS2	-	-89.2	-	dBm
	MCS3	-	-86.1	-	dBm
	MCS4	-	-82.5	-	dBm

GI and non-STBC	MCS5	-	-77.9	-	dBm
	MCS6	-	-76.3	-	dBm
	MCS7	-	-74.7	-	dBm
RX sensitivity IEEE 802.11n (10% PER for 4096 octet PSDU) Defined for default parameters : 800 ns GI and non-STBC	40 MHz channel spacing for all MCS rates	-		-	
	MCS0	-	-91.8	-	dBm
	MCS1	-	-88.9	-	dBm
	MCS2	-	-86.5	-	dBm
	MCS3	-	-83.0	-	dBm
	MCS4	-	-79.9		dBm
	MCS5		-75.2	-	dBm
	MCS6	-	-73.7	-	dBm
	MCS7	-	-72.3	-	dBm
RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) Defined for default parameters : 800 ns GI and non-STBC	20 MHz channel spacing for all MCS rates				
	MCS0	-	-93.3	-	dBm
	MCS1	-	-90.3	-	dBm
	MCS2	-	-87.9	-	dBm
	MCS3	-	-84.9	-	dBm
	MCS4	-	-81.4	-	dBm
	MCS5	-	-76.7	-	dBm
	MCS6	-	-75.7	-	dBm
	MCS7	-	-74.6	-	dBm
	MCS8	-	-70.2	-	dBm
RX sensitivity IEEE 802.11ac (10% PER for 4096 octet PSDU) Defined for default parameters : 800 ns GI and non-STBC	40 MHz channel spacing for all MCS rates				
	MCS0	-	-90.5		dBm
	MCS1		-87.4	-	dBm
	MCS2	-	-85.3	-	dBm
	MCS3	-	-82.1	-	dBm
	MCS4	-	-79	-	dBm
	MCS5	-	--73.9	-	dBm
	MCS6	-	-72.4	-	dBm
	MCS7	-	-72.3		dBm
	MCS8		-67.9		dBm
	MCS9		-66.6		dBm
RX sensitivity IEEE 802.11ac	80 MHz channel spacing for all MCS rates				
	MCS0	-	-87	-	dBm

(10% PER for 4096 octet PSDU) Defined for default parameters : 800 ns GI and non-STBC	MCS1	-	-83.9	-	dBm
	MCS2	-	-81.9	-	dBm
	MCS3	-	--78.1	-	dBm
	MCS4	-	-75	-	dBm
	MCS5	-	-73	-	dBm
	MCS6	-	-68.5	-	dBm
	MCS7	-	-68.5	-	dBm
	MCS8	-	-64.3	-	dBm
	MCS9	-	-62.7	-	dBm
Maximum receiver level@ 5.24 GHz	@ 6, 9, 12 Mbps	-9.5	-	-	dBm
	@ 18, 24, 36, 48, 54 Mbps	-14.5	-	-	dBm
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified)	6 Mbps OFDM -79dBm	16	-	-	dB
	9 Mbps OFDM -78dBm	15	-	-	dB
	12 Mbps OFDM -76dBm	13	-	-	dB
	18 Mbps OFDM -74dBm	11	-	-	dB
	24 Mbps OFDM -71dBm	8	-	-	dB
	36 Mbps OFDM -67dBm	4	-	-	dB
	48 Mbps OFDM -63dBm	0	-	-	dB
	54 Mbps OFDM -62dBm	-1	-	-	dB
	65 Mbps OFDM -61dBm	-2	-	-	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified)	6 Mbps OFDM -78.5dBm	32	-	-	dB
	9 Mbps OFDM -77.5dBm	31	-	-	dB
	12 Mbps OFDM -75.5dBm	29	-	-	dB
	18 Mbps OFDM -73.5dBm	27	-	-	dB
	24 Mbps OFDM -70.5dBm	24	-	-	dB
	36 Mbps OFDM -66.5dBm	20	-	-	dB
	48 Mbps OFDM -62.5dBm	16	-	-	dB
	54 Mbps OFDM -61.5dBm	15	-	-	dB
	65 Mbps OFDM -60.5dBm	14	-	-	dB

10.4.2 WLAN 5 GHz Transmitter Characteristics

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Tx power at Antenna port for highest power level setting at 25 °C and VDD = 3.3 V with spectral mask and EVM compliances	OFDM, QPSK -13 dB	-	19	-	dBm
	OFDM, 16-QAM -19 dB	-	16	-	dBm
	OFDM, 64-QAM -25 dB (R = 3/4)	-	16	-	dBm
	OFDM, 16-QAM -27 dB (MCS7, HT20)	-	16	-	dBm
	OFDM, 16-QAM -30 dB (MCS8, HT80)	-	14	-	dBm
	OFDM, 16-QAM -32 dB (MCS9, VHT40 And VHT80)	-	14	-	dBm

10.4.3 WLAN 2.4 GHz Receiver Characteristics

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	-	2400	-	2500	MHz
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	-	-98.4	-	dBm
	2 Mbps DSSS		-96.5		dBm
	5.5 Mbps DSSS		-93.7		dBm
	11 Mbps DSSS		-91.4		dBm
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps OFDM		-95.5		dBm
	9 Mbps OFDM		-94.1		dBm
	12 Mbps OFDM		-93.2		dBm
	18 Mbps OFDM		-90.6		dBm
	24 Mbps OFDM		-87.3		dBm
	36 Mbps OFDM		-84.0		dBm
	48 Mbps OFDM		-79.3		dBm
	54 Mbps OFDM		-77.8		dBm
RX sensitivity IEEE 802.11n (10% PER for 4096octet PSDU) Defined for default parameters : 800 ns	20 MHz channel spacing for all MCS rates				
	MCS0		-94		dBm
	MCS1		-91.7		dBm
	MCS2		-89.2		dBm
	MCS3		-86.1		dBm
	MCS4		-82.5		dBm

GI and non-STBC	MCS5		-77.9		dBm
	MCS6		-76.3		dBm
	MCS7		-74.7		dBm
RX sensitivity IEEE 802.11n (10% PER for 4096octet PSDU) Defined for default parameters : 800 ns GI and non-STBC	40 MHz channel spacing for all MCS rates				
	MCS0		-94		dBm
	MCS1		-91.7		dBm
	MCS2		-89.2		dBm
	MCS3		-86.1		dBm
	MCS4		-82.5		dBm
	MCS5		-77.9		dBm
	MCS6		-76.3		dBm
	MCS7		-74.7		dBm

10.4.4 WLAN 2.4 GHz Transmitter Characteristics

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Tx power at Antenna port for highest power level setting at 25 °C and VDD = 3.3 V with spectral mask and EVM compliances	802.11b -9 dB		19		dBm
	OFDM, BPSK -8 dB		17		dBm
	OFDM, QPSK -13 dB		17		dBm
	OFDM, 64-QAM -19 dB		16		dBm
	OFDM, 64-QAM -25 dB (R = 3/4)		16		dBm
	OFDM, 64-QAM -27 dB (MCS7, HT20)		16		dBm
	OFDM, 256-QAM -30 dB (MCS8, VHT20)		14		dBm
	OFDM, 256-QAM -32 dB (MCS8, VHT40)		14		dBm

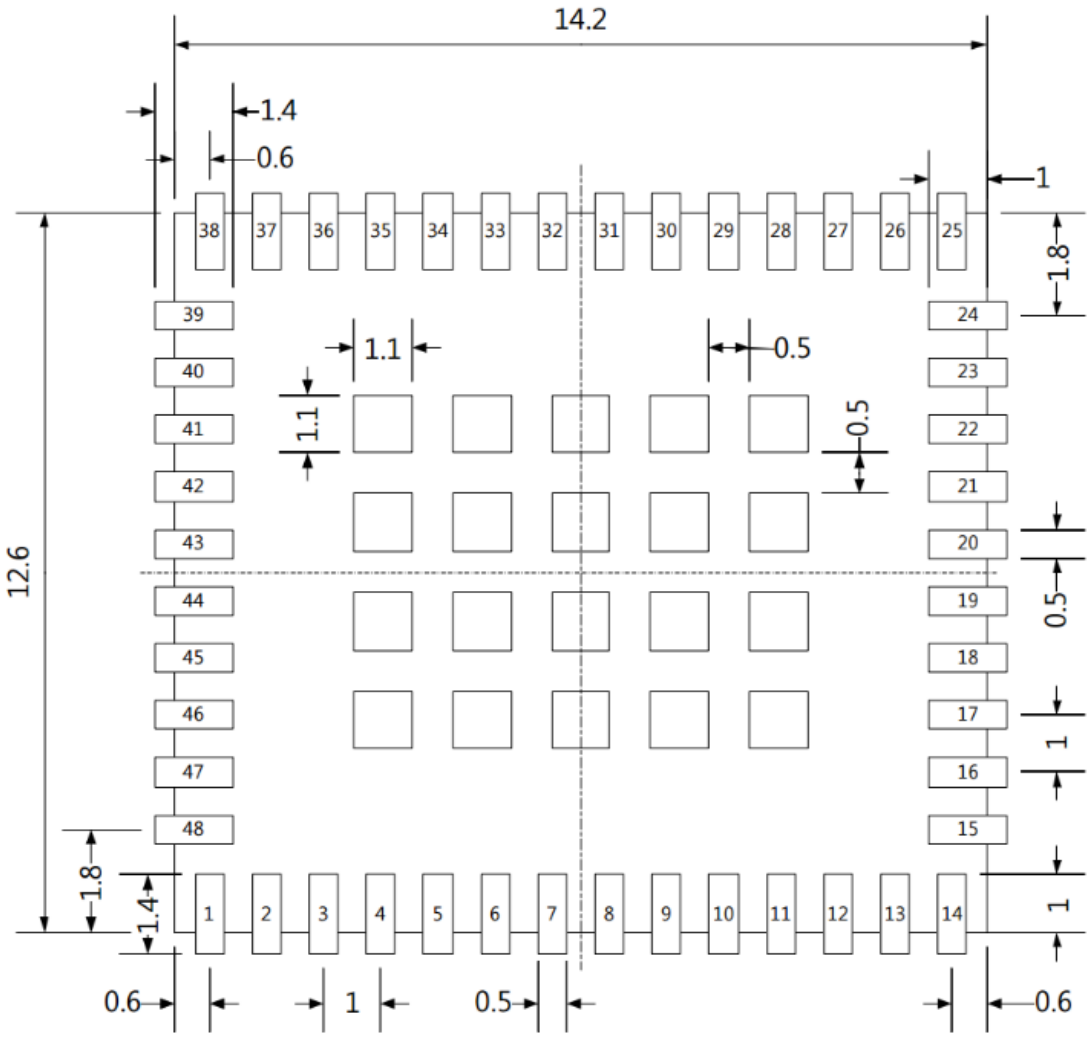
10.4.5 BT RF Characteristics

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range		2402	-	2480	MHz
RX sensitivity	GFSK, 0.1% BER, 1 Mbps	-	-90.5	-	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	-	-92.5	-	dBm
	8-DPSK, 0.01% BER, 3 Mbps	-	-86.5	-	dBm
Basic rate (GFSK) TX Power		9	11		dBm
QPSK TX Power		6	8		dBm
8PSK TX Power		6	8		dBm
Power control step		2	4	8	dB

10.4.6 BLE RF Characteristics

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range		2402	-	2480	MHz
RX sense	GFSK, 0.1% BER, 1 Mbps		-92.5		dBm
TX power		-	6.5	-	dBm
Mod Char : delta F1 average		225	255	275	kHz
Mod Char : delta F2 max		99.9	-	-	%
Mod Char : ratio		0.8	0.95	-	%

11. Reference metal paste pattern



Above figure shows the PCB land pattern used for the module evaluation board. When the module is mounted on the evaluation board, solder mask with 0.12 mm thickness is used. The solder paste mask is the same dimension as the PCB land pattern.

This land pattern is preliminary information, then may be changed due to further evaluation. Once it should be changed, F1media will inform the updated land pattern.