F1BD89C1

Data sheet

Confidential / Preliminary Documentation

Revision 1.3

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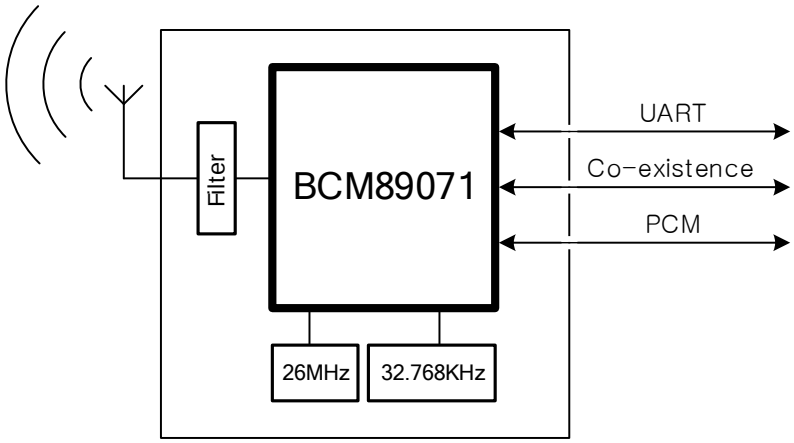
List of Contents

1. General

1.1 overview

The F1BD89C1 complies with the Bluetooth Core Specification, version 4.1 and is designed for use with a standard Host Controller Interface (HCI) UART. All detailed specification including pinouts and electrical specification may be changed without notice.



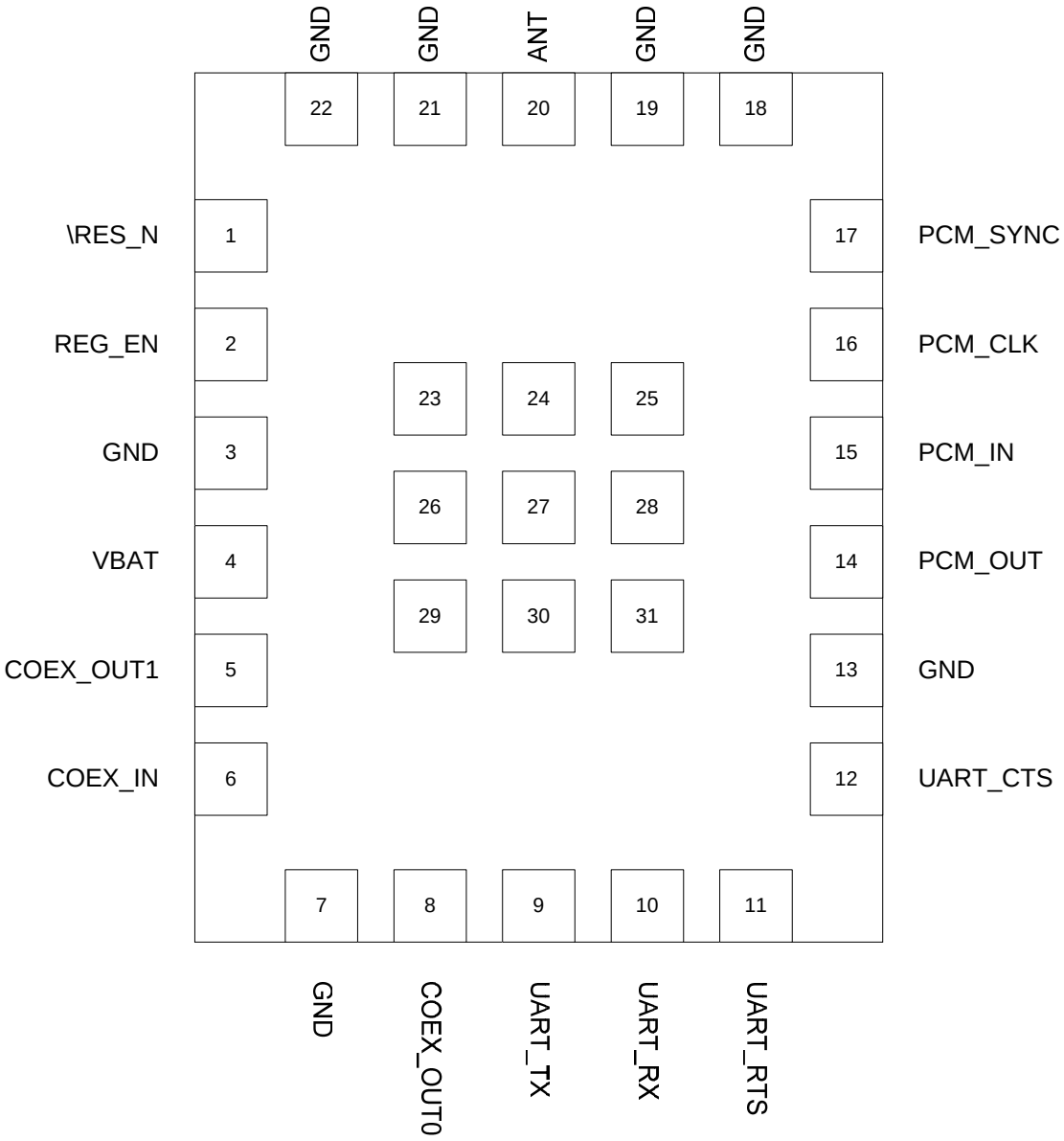
1.2 Features

- Bluetooth 4.1 + EDR
- Full support power saving modes
  - Bluetooth standard Hold and sniff
  - Deep sleep modes and regulator shutdown
- Support for 802.11 Co-existence (3-wire)
- Supports maximum Bluetooth data rates over HCI UART interface
- Multipoint operation, with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO links, with Scatternet support
- Scatternet operation, with up to four active piconets (with background scan and support for scatterMode)
- RoHS Compliant
- Supports Wide-Band Speech (WBS) over PCM and Packet Loss Concealment (PLC) for better audio quality
- Competitive Size (11mm x 13mm x 2.0mm : QFN 22Pin)

1.3 Application

- Automotive hands-free radios
- Automotive data communication

1.4 Pin out Diagram

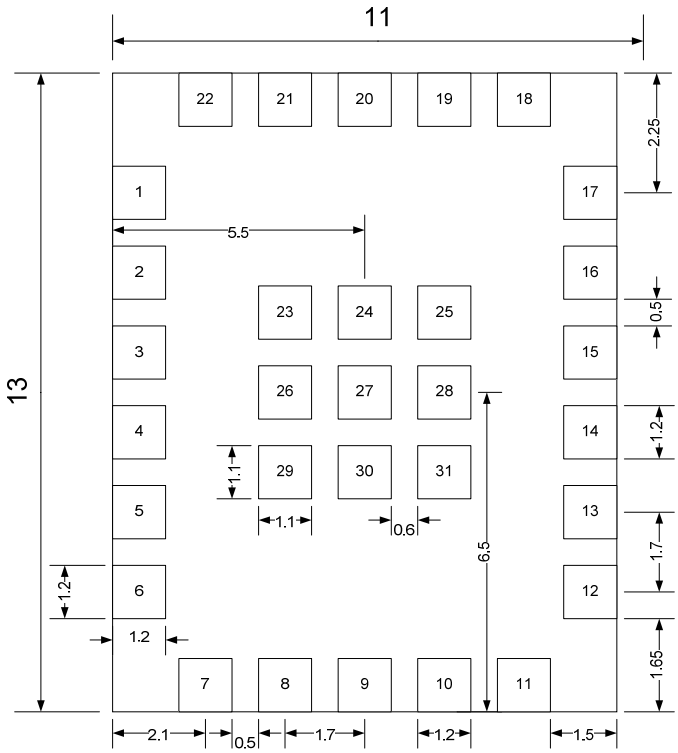


< Top View >

1.5 Device Terminal Functions

	PIN	Name	Description
PCM	PCM_OUT	14	PCM/I2S data output
	PCM_IN	15	PCM/I2S data input
	PCM_CLK	16	PCM/I2S clock
	PCM_SYNC	17	PCM sync / I2S word select
UART	UART_TX	9	
	UART_RX	10	
	UART_CTS	12	
	UART_RTS	11	
Co-existence	BT_STATUS	5	
	WLAN_ACT	6	3-Wire Co-existence
	BT_ACT	8	
Other Pins	ANT	20	RF Connection to Antenna
	GND	3,7,13,18,19,21,22	Ground
	VBAT	4	LDO input
	REG_EN	2	LDO Enable
	/RES_N	1	Active low reset input

1.6 Module Dimension (Top view)



2. Characteristics

2.1 Electrical Characteristics

Absolute Maximum Ratings

Rating	Minimum	Maximum
Storage temperature	-40°C	85°C
Max Junction Temperature(Tjmax)		125°C
Supply voltage : VBAT	2.5V	3.6V

Recommended Operating Conditions

Operating Condition	Minimum	Maximum
Operating temperature range	-30°C	85°C
Supply voltage : VCC	3.0V	3.3V

2.2 RF Characteristics

Transmitter

Specification	Condition	Min	Typ	Max	Unit
Output transmit power	Normal	-6	1	4	dBm
Transmit power density	Normal			4	dBm
Transmit power control	Normal	2		8	dBm
Frequency Range	Normal	2400		2483.5	MHz
20dB bandwidth for modulated carrier	Normal		850	1000	KHz
Adjacent channel transmit power	±2MHz ±3MHz ±4MHz			-20 -40 -40	dBm
Modulation Characteristics	f1avg f2max f2avg / f1avg	140 115		175 80	KHz KHz %
Initial carrier frequency tolerance	Normal	-20		20	KHz
Carrier frequency Drift	One slot packet(DH1) Three slot packet(DH3) Five slot packet(DH5)	-25 -40 -40		25 40 40	KHz

Transceiver

Specification	Condition	Min	Typ	Max	Unit
Adjacent channel transmit power	30MHz ~ 1GHz 1GHz ~12.75GHz 1.8GHz ~5.1GHz 5.1GHz ~5.3GHz			-36 -30 -47 -47	dBm

Receiver

Specification	Condition	Min	Typ	Max	Unit
Sensitivity level (0.1% BER)	Single slot packets	-70	-80		dBm
Transmit power density	Multi slot packet	-70	-80		dBm
C/I performance	co-channel 1MHz (Adjacent channel) 2MHz (2nd Adjacent channel) 3MHz (3rd Adjacent channel)			11 0 -30 -40	dB
Blocking performance	30MHz ~ 2000MHz 2000MHz ~ 2400MHz 2500MHz ~ 3000MHz 3000MHz ~ 12.75GHz	-10 -27 -27 -10			dBm
Intermodulation performance	n=5	-39			dBm
Maximum input level		-20	-10		dBm

3. Terminal Description

3.1 UART

The UART physical interface is standard, 4-wire interface (RX,TX,RTS,CTS) with adjustable baud rates from 9600 bps to 4.0Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate can be selected via a vendor-specific UART HCI command. The interface supports Bluetooth UART HCI (H4) specifications. The default baud rate for H4 is 115.2Kbaud.

The following baud rates are supported :

- 9600
- 14400
- 19200
- 28800
- 38400
- 57600
- 115200
- 230400
- 460800
- 921600
- 1444444
- 1500000
- 2000000
- 3000000
- 3250000
- 3692000
- 4000000

Normally, the UART baud rate is set by a configuration record downloaded after reset or by automatic baud rate detection. The host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is provided through a vendor-specific command.
The F1BD89C1 UART operates with the host UART correctly, provided the combined baud rate error of the two devices is within ± 2%

HCI 3-Wire Transport (UART H5)

The F1BD89C1 support H5 UART transport for serial UART communications. H5 reduces the number of signal lines required by eliminating CTS and RTS, when compared to H4. In addition, in-band sleep signaling is supported over the same interface so that the 4-wire UART and the 2-wire sleep signaling interface can be reduced to a 2-wire UART interface, saving four IOs on the host.

H5 requires the use of an external LPO. CTS must be pulled low.

3.2 PCM interface

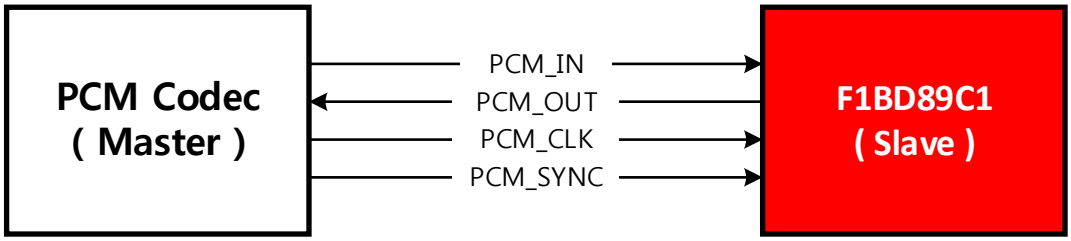
THE F1BD89C1 PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, the device generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface as inputs to the device.

The device supports up to three SCO and eSCO channels through the PCM interface and each channel can be independently mapped to any available slot in a frame.

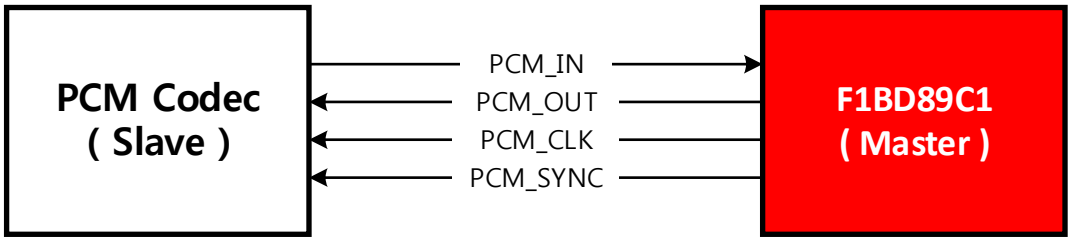
The host can adjust the PCM interface configuration using vendor-specific HCI commands or it can be setup in the configuration file.

System Diagram

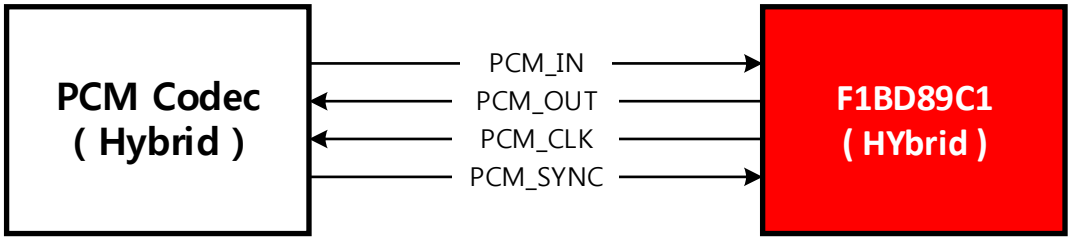
PCM interface with Linear PCM Coded



PCM interface Slave Mode



PCM interface Master Mode



PCM interface Hybrid Mode

Slot Mapping

The device supports up to three simultaneous, full duplex SCO or eSCO channels. These channels are time-multiplexed onto the PCM interface using a time slotting scheme based on the audio sapling rate, as described in table 1

Table 1 : PCM interface Time Slotting Scheme

Audio Sample Rate	Time Slotting Scheme	
8KHz	The number of slots depends on the selected interface rate, as follows :	
	Interface rate	**Slot**
	128	1
	256	2
	512	4
	1024	8
	2048	16
16KHz	The number of slots depends on the selected interface rate, as follows :	

Interface rate	Slot
256	1
512	2
1024	4
2048	8

Transmit and receiver PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Wideband Speech

The F1BD89C1 provides support for Wideband Speech (WBS) in two ways :

- Transparent mode : The host encodes WBS packets and the encoded packets are transferred over the master mode for a 4KHz sync rate with 16-bit samples, resulting in a 64kbps bit rate.
- On-chip SmartAudio technology : The F1BD89C1 can perform SBC encoding and decoding of linear 16 bits at 16kHz (256kbps rate) transferred over the PCM bus.

Frame Synchronization

The device supports both short and long frame synchronization types in both master and slave configurations. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8kHz audio frame rate (which is a single bit period in width) and synchronized to the rising edge of the bit clock. The PCM slave expects PCM_SYNC to be high on the falling edge of the bit clock and the first bit of the first slot to start at the next rising edge of the clock. In the long frame synchronization mode, the frame synchronization signal is and active high pulse at the 8kHz audio frame rate. However, the duration is 3-bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The device can he configured to generate and accept several different data formats. The device uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits is configurable to support various data formats on the PCM interface. The remaining three bits are ignored on the input, and may be filled with zeros, ones, a sign bit, or a programmed value on the output. The default format is 13-bit two's complement data, left justified, and clocked most significant bit first.

3.3 HCI Transport Detection Configuration

The F1BD89C1 supports the following interface types for the HCI transport from the host :

- UART (H4 and H5)

Only one host interface can be active at a time. The firmware performs a transport detect function at boot-time to determine which host is the active transport. It can auto-detect the UART interface.

4. Timing Description

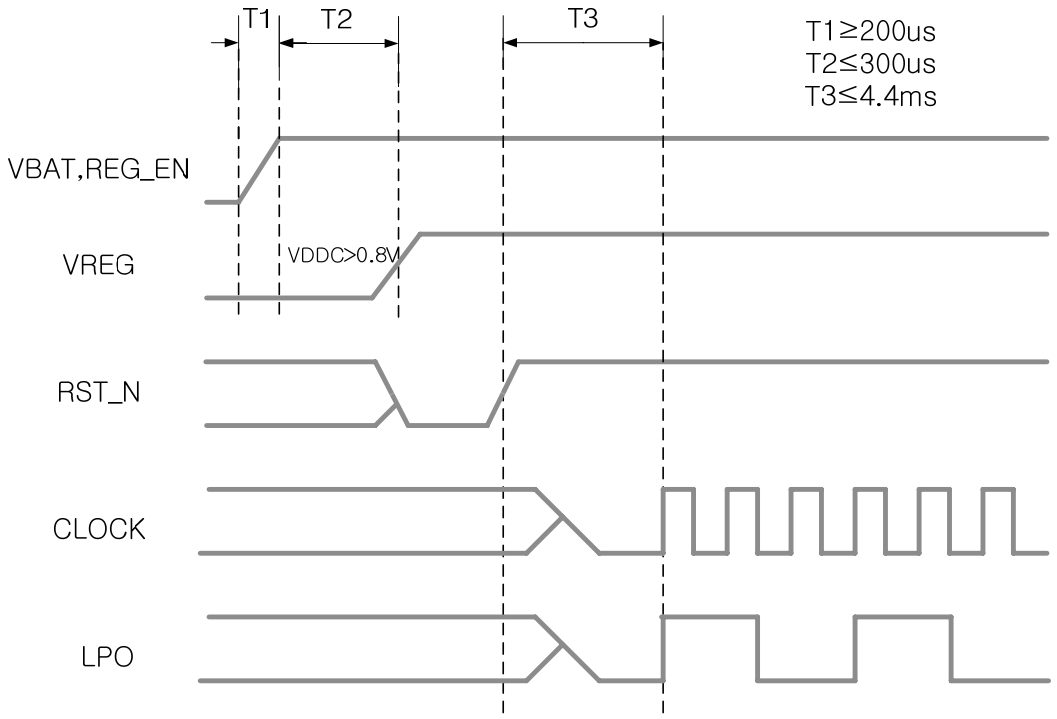
4.1 Startup Timing

There are two basic startup scenario.

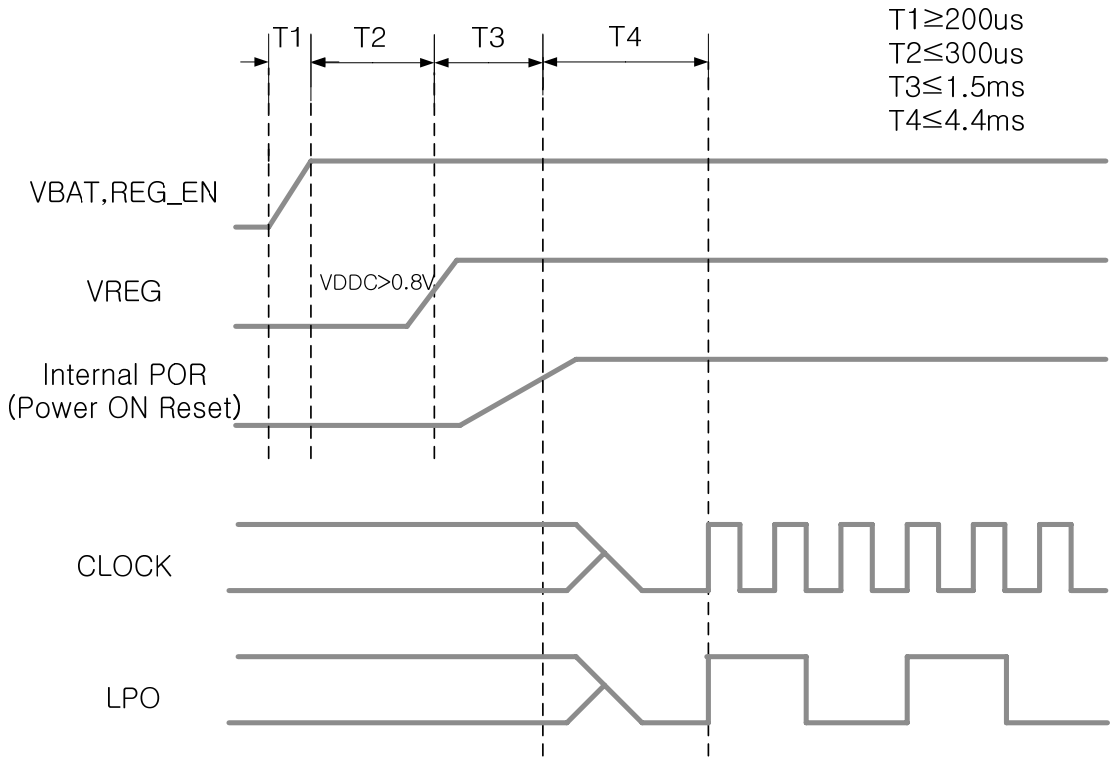
- The chip startup and firmware boot is held off while the RST_N pin is asserted.
- The Chip Startup and firmware boot is directly triggered by the chip power-up.

  In this case, an internal power-on reset(POR) is held for a few ms, after which the chip commences startup.

4.1.1 Startup Timing from RST_N

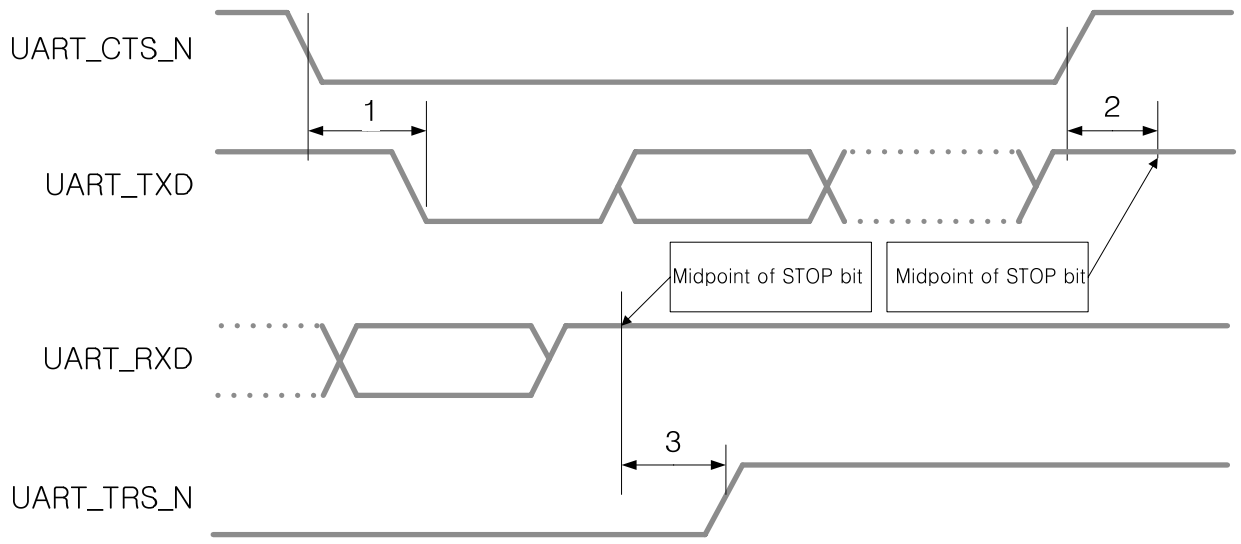


4.1.2 Startup Timing from Power-on Reset



4.2 UART Timing

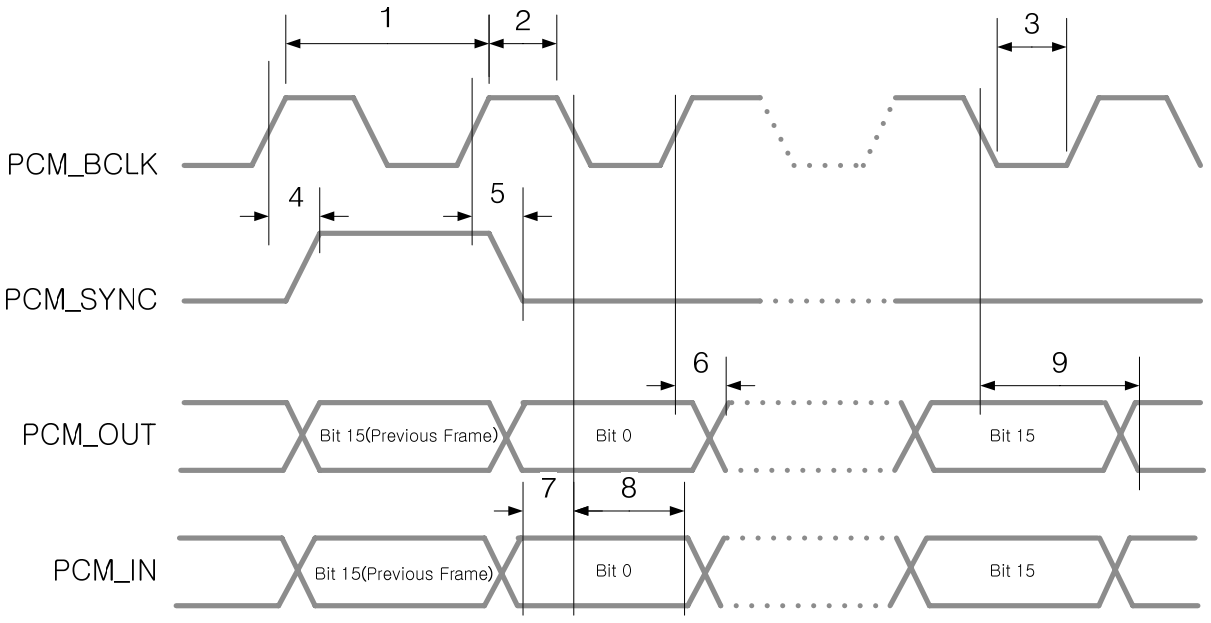
Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	-	24	Baudout cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	2	Baudout cycles



4.3 PCM Interface Timing

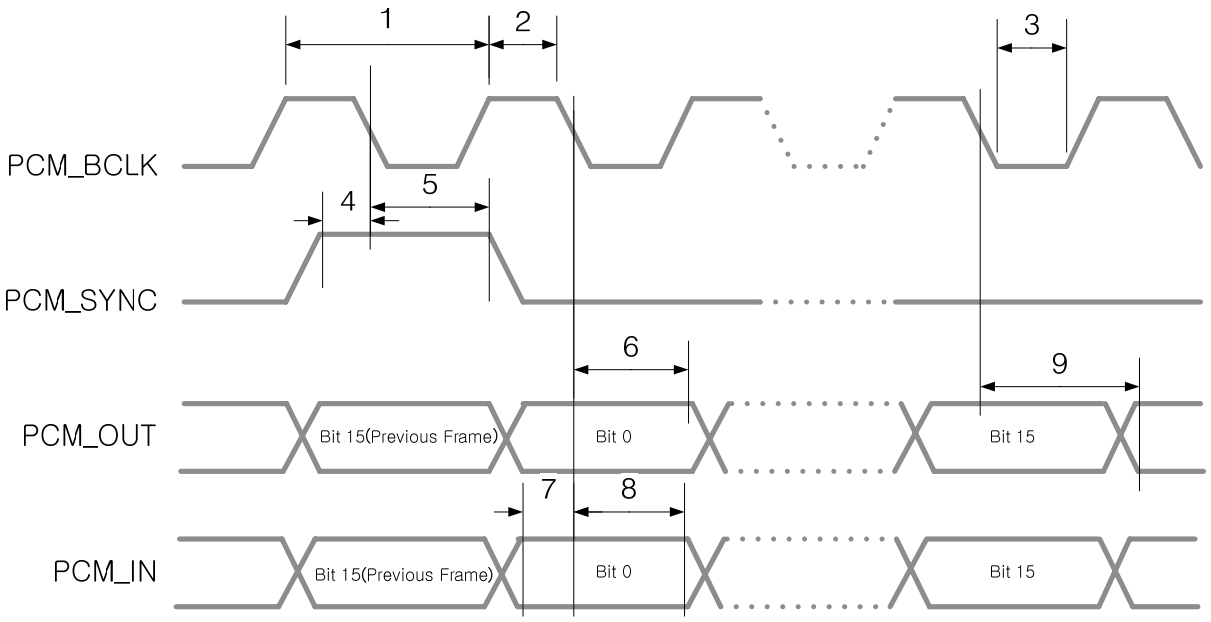
4.3.1 PCM Interface Timing(Short Frame Synchronization, Master Mode)

Reference	Characteristics	Min	Max	Unit
1	PCM bit clock frequency	128	2048	KHz
2	PCM bit clock HIGH time	128	-	ns
3	PCM bit LOW time	209	-	ns
4	Delay from PCM_BCLK rising edge to PCM_SYNC high	-	50	ns
5	Delay from PCM_BCLK rising edge to PCM_SYNC low	-	50	ns
6	Delay from PCM_BCLK rising edge to data valid on PCM_OUT	-	50	ns
7	Setup time for PCM_IN before PCM_BCLK falling edge	50	-	ns
8	Hold time for PCM_IN after PCM_BCLK falling edge	10	-	ns
9	Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	-	50	ns



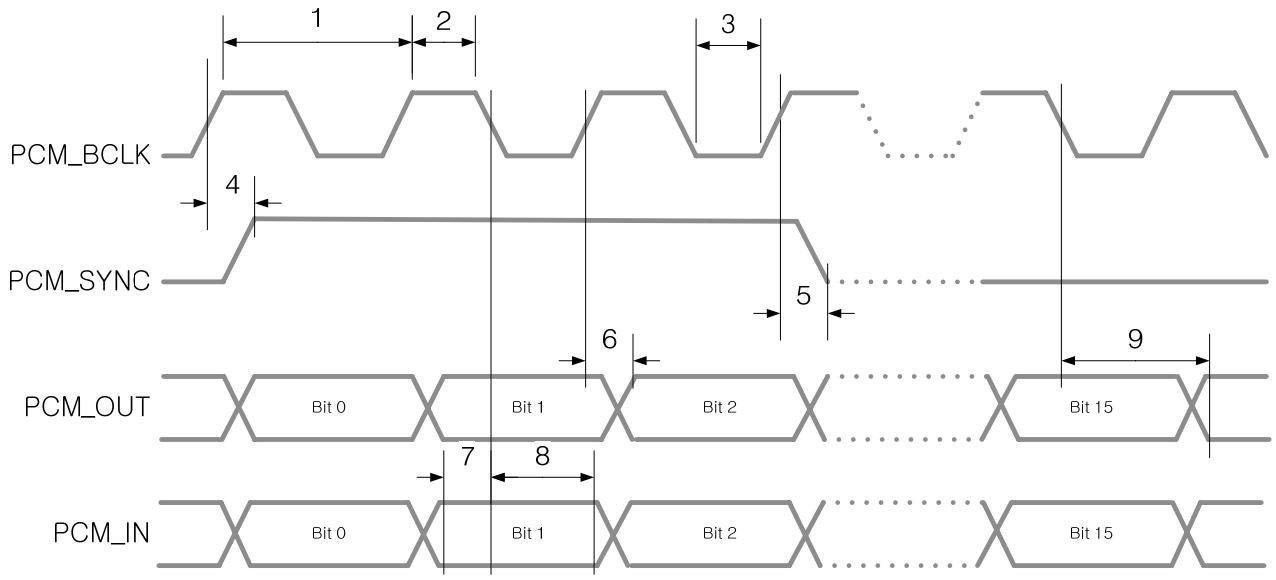
4.3.2 PCM Interface Timing(Short Frame Synchronization, Slave Mode)

Reference	Characteristics	Min	Max	Unit
1	PCM bit clock frequency	128	2048	KHz
2	PCM bit clock HIGH time	209	-	ns
3	PCM bit LOW time	209	-	ns
4	Setup time for PCM_SYNC before falling of PCM_BCLK	-	50	ns
5	Hold time for PCM_SYNC after falling edge of PCM_BCLK	-	50	ns
6	Hold time of PCM_OUT after PCM_BCLK falling edge	-	50	ns
7	Setup time for PCM_IN before PCM_BCLK falling edge	50	-	ns
8	Hold time for PCM_IN after PCM_BCLK falling edge	10	-	ns
9	Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	-	50	ns



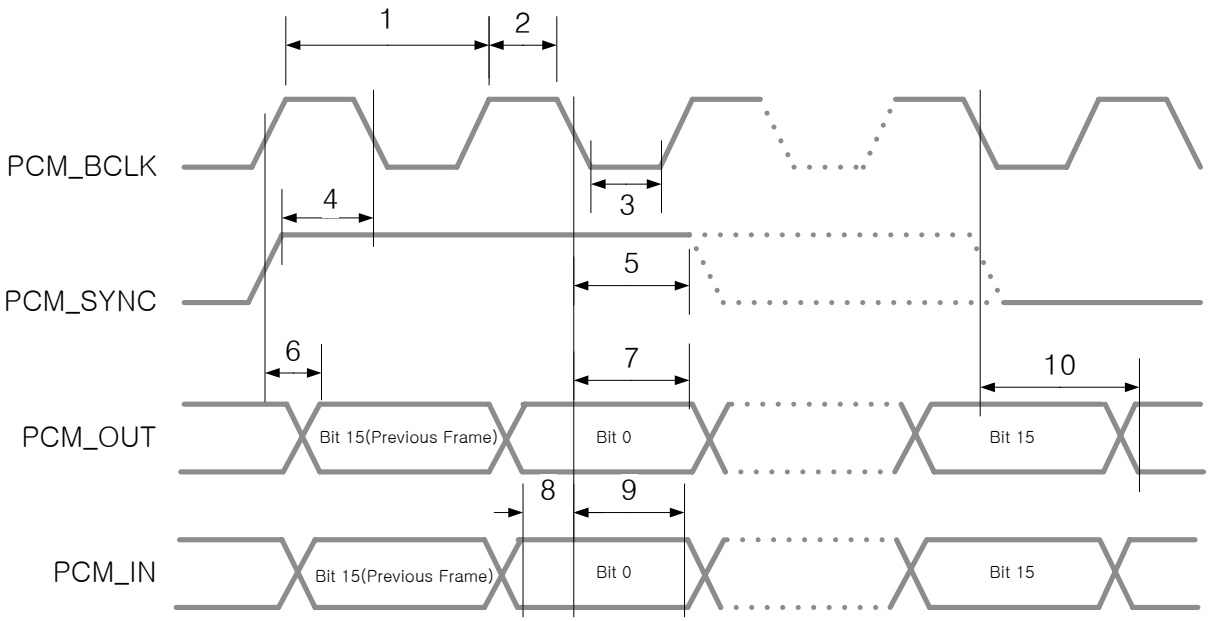
4.3.3 PCM Interface Timing(Long Frame Synchronization, Master Mode)

Reference	Characteristics	Min	Max	Unit
1	PCM bit clock frequency	128	2048	KHz
2	PCM bit clock HIGH time	209	-	ns
3	PCM bit LOW time	209	-	ns
4	Delay from PCM_BCLK rising edge to PCM_SYNC HIGH during first bit time	-	50	ns
5	Delay from PCM_BCLK rising edge to PCM_SYNC LOW during third bit time	-	50	ns
6	Delay from PCM_BCLK rising edge to data valid on PCM_OUT	-	50	ns
7	Setup time for PCM_IN before PCM_BCLK falling edge	50	-	ns
8	Hold time for PCM_IN after PCM_BCLK falling edge	10	-	ns
9	Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	-	50	ns

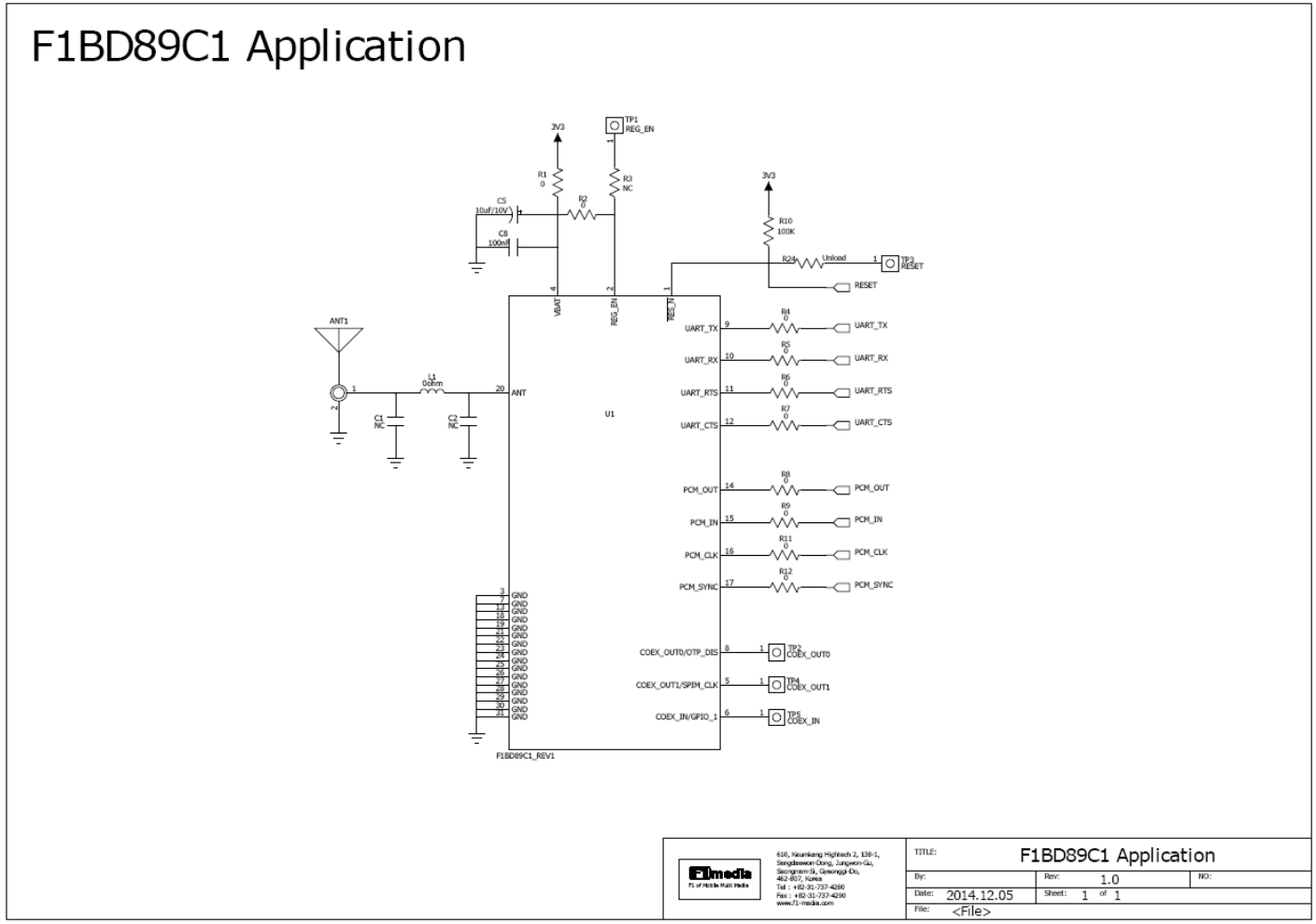


4.3.4 PCM Interface Timing(Long Frame Synchronization, Slave Mode)

Reference	Characteristics	Min	Max	Unit
1	PCM bit clock frequency	128	2048	KHz
2	PCM bit clock HIGH time	209	-	ns
3	PCM bit LOW time	209	-	ns
4	Setup time for PCM_SYNC before falling edge of PCM_BCLK during first bit time	-	50	ns
5	Hold time for PCM_SYNC after falling edge of PCM_BCLK during second bit period.(PCM_SYNC may go low any time from second bit period to last period)	-	50	ns
6	Hold time of PCM_OUT after PCM_BCLK falling edge	-	175	ns
7	Setup time for PCM_IN before PCM_BCLK falling edge	50	-	ns
8	Hold time for PCM_IN after PCM_BCLK falling edge	10	-	ns
9	Delay from falling edge of PCM_BCLK or PCM_SYNC(whichever is later)during last bit in slot to PCM_OUT becoming high impedance.	-	100	ns

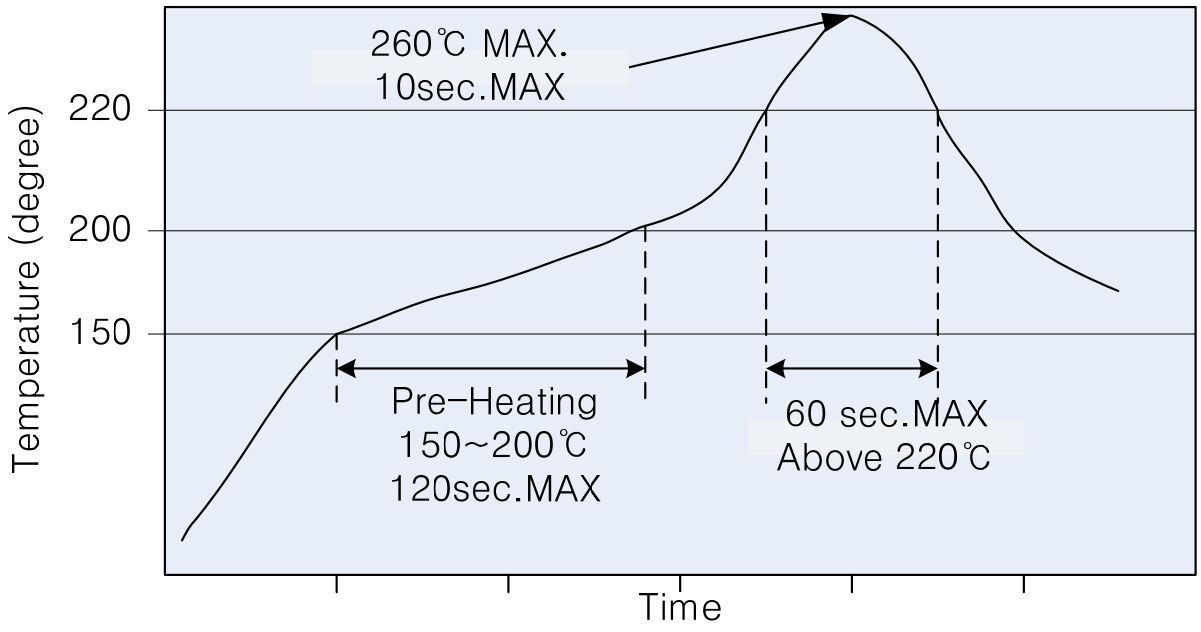


5. Application Schematic



6. Reflow Temperature Profile

Recommended solder reflow profile are shown in below and follow the lead-free profile in accordance with JEDEC Std 20C. Table lists the critical reflow temperatures. Flux residue remaining from board assembly can contribute to electrochemical migration (ECM) over time. This depends on a number of factors, including flux type, amount of flux residue remaining after reflow, and stress conditions during product use, such as temperature, humidity, and potential difference between pins. Care should be taken in selecting production board/module assembly processes and materials, taking into account these factors.



Process Step	Lead-Free Solder
Pre-Heat	150~200°C
Pre-Heat Time	MAX 120 sec.
Time above liquidus	Above +220°C. MAX 60 sec
Peak temperature	MAX +260°C
Time within 5°C of peak temperature	MAX 10 sec

7. Revision History

Revision	Date	Change Descriptions	Issued by
Rev 1.0	2015.2.27	Initial release	landrover
Rev 1.1	2015.03.09	Timing update	JM.KWON
Rev 1.2	2015.04.30	Data update	JM.KWON
Rev 1.3	2016.04.12	Junction Temperature Add	JH.Park