SYD8801: Low Power Bluetooth 4.0 Single Mode SOC

1.1 General Description

The SYD8801 is a low power and high performance 2.4GHz Bluetooth Low Energy SOC. This SOC integrates all the essentials of a Bluetooth smart device which includes 32-bit ARM Cortex-M0 with Flash memory, digital interface support and high performance 2.4GHz RF transceiver. A built-in DCDC converter is included to provide a complete low power SOC solution for stand-alone applications such as HID and Wearable devices.

1.2 Key Features

- Fully qualified Bluetooth Low Energy 4.0 peripheral device
- Up to 98dBm link budget
- Sub 10mA TRx radio current
- Cortex M0 32-bit MCU with max. 32MHz clock rate
- Low power and excellent performance 2.4GHz transceiver with built-in balun for compact layout area and low BOM cost;
- 2 channel 10-bit SAR ADC
- Highly integrated SOC with 128kB Flash and 80kB SRAM
- 16MHz and 32.768kHz crystal oscillator circuit with on-chip loading capacitors, no external loading capacitors needed
- Quadrature Decoder
- DCDC converter, Boost or Buck Mode
- Built in 32MHz and 32.768kHz RC oscillator
- Communication interface options
  - Master I2C x2
  - Master Two/Four-Wire SPI x2
  - UART x2
- Digital peripherals
  - LED x3
  - PWM x3
- Support Serial Wire (SW) debug mode
-

1.3 Applications

- Wearable device (wristband, smart watch, etc.)
- HID device (smart remote controller, etc.)
- BLE module (UART transmission)
- Health applications (smart weight, etc.)
- Home and industrial automation

1.4 Key Parameters

Parameter	Value
Max. TX Power	+4 dBm
RX Sensitivity	-94 dBm
TX RF Current @0dBm*	7.1 mA
RX RF Current @sensitivity level*	8.2 mA
Sleep Mode Current	<7.5 µA
Deep Sleep Mode Current	<2.5 µA
RF Input Impedance	50 Ω
ROM Size	24 kB
Internal Flash	128 kB
SRAM	80 kB
Supply Voltage	Buck Mode: 1.9~3.6 V
GPIO	30
Operating Temperature, Tj	-40~+85 °C

*Measured under DCDC Mode @V_{BAT}=3V

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MENU

2.0 Introduction

2.1 Overview

The SYD8801 chip is highly integrated with ARM® Cortex®-M0 processor, Bluetooth Low Energy v4.0 baseband control core, ROM, Flash, Bluetooth Modem, Radio Transceiver, on-chip Balun and digital interfaces for the BLE application. The Cortex M0 can operate at 32MHz clock rate for heavy thread computing application, and can also operate at lower clock rate for simple data communication purpose. SYD8801 has DCDC converter built-in to provide full-solution SoC for stand-alone applications such as HID and Wearable devices.

Figure 1 shows the architecture block diagram of the chip. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

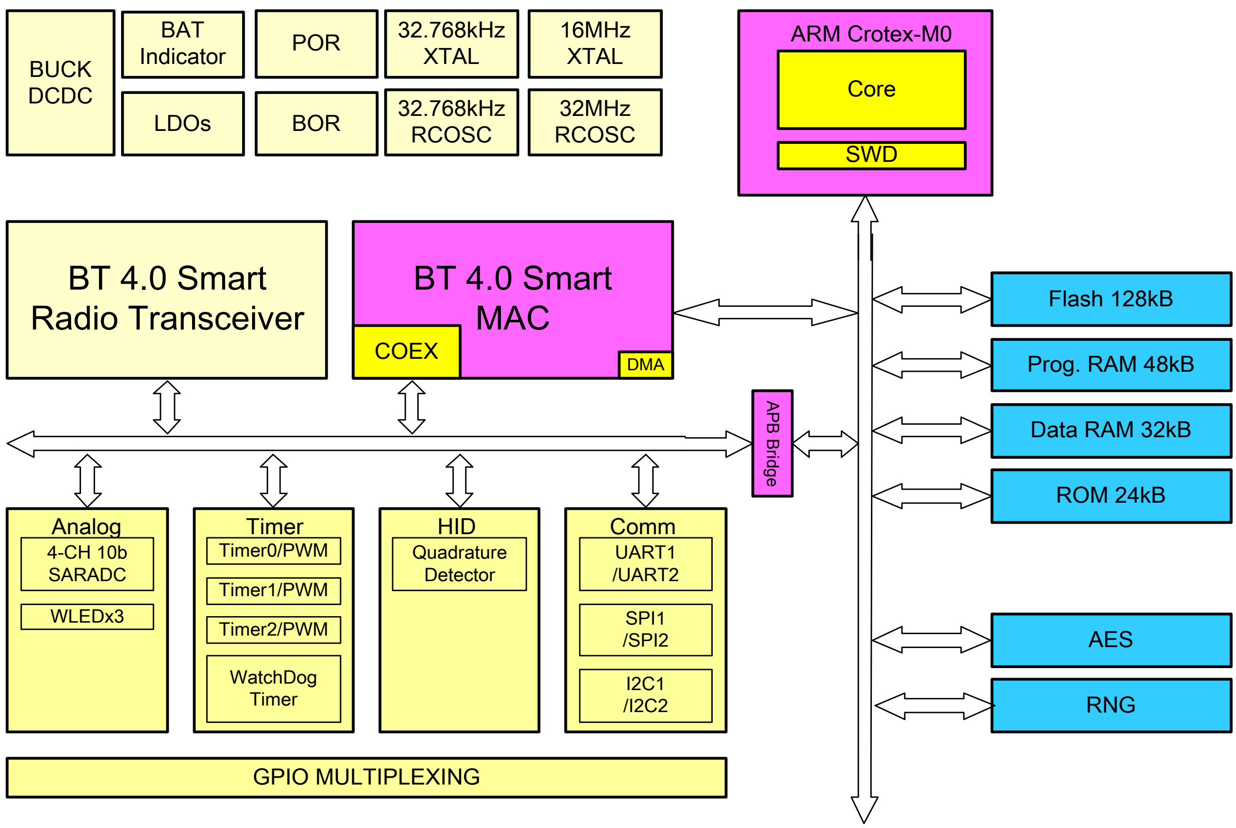


Figure 1. Functional Block Diagram

2.2 Terminology

Term	Description
GND	Ground
BiDir	Bi-Directional
PWM	Pulse Width Modulation
HID	Human Interface Device
GPIO	General Purpose Input / Output

2.3 Pin Assignment and Signal Description

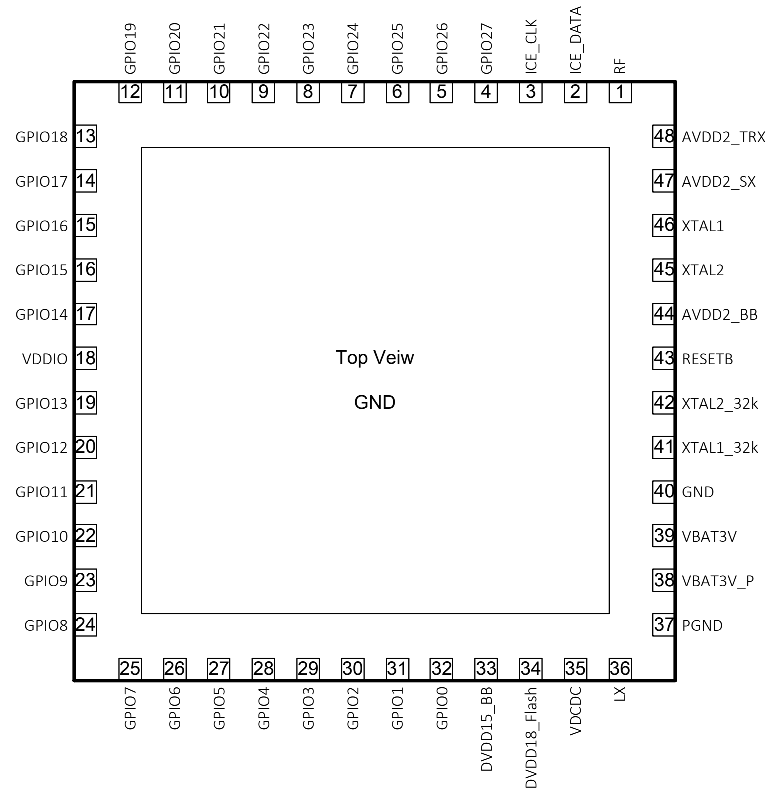


Figure 2. Pin Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
1	RF	BiDir	2.4GHz transceiver RF port, connected to antenna
2	ICE_DATA	BiDir	PWM0, or LED0 Serial debug port interface – DATA
3	ICE_CLK	BiDir	PWM1, or LED1 Serial debug port interface – Clock
4	GPIO27	BiDir	GPIO, PWM2, or LED2 I^2C: Data IO, as I2C_SDA0 UART: UART_TXD0
5	GPIO26	BiDir	GPIO, PWM0, or LED0 I^2C:Clock output, as I2C_SCL0, UART: UART_RXD0
6	GPIO25	BiDir	GPIO, Key_T2, PWM1, or LED1 UART: UART_RTS0
7	GPIO24	BiDir	GPIO, Key_T1, PWM2, or LED2 UART: UART_CTS0

Pin No.	Signal Name	Type	Description
8	GPIO23	BiDir	GPIO, or Key_Z2 I^2C: Data IO, as I2C_SDA1 UART: UART_TXD1
9	GPIO22	BiDir	GPIO, or Key_Z1 I^2C:Clock output, I2C_SCL1 UART: UART_RXD1
10	GPIO21	BiDir	GPIO, PWM1, or LED1
11	GPIO20	BiDir	GPIO, PWM2, or LED2 UART: UART_TXD0
12	GPIO19	BiDir	GPIO, PWM0, or LED0 UART: UART_RXD0
13	GPIO18	BiDir	GPIO, PWM1, or LED1 UART: UART_RTS0
14	GPIO17	BiDir	GPIO, PWM2, or LED2 UART: UART_CTS0
15	GPIO16	BiDir	GPIO, PWM0, or LED0 I^2C:Data IO, I2C_SDA1
16	GPIO15	BiDir	GPIO, PWM1, or LED1 I^2C:Clock output, I2C_SCL1
17	GPIO14	BiDir	GPIO, PWM2, or LED2
18	VDDIO	Power	Power for IO, 1.8V~3.3V
19	GPIO13	BiDir	GPIO
20	GPIO12	BiDir	GPIO
21	GPIO11	BiDir	GPIO
22	GPIO10	BiDir	GPIO
23	GPIO9	BiDir	GPIO SPI4W: Master, Data output, SPI_DO
24	GPIO8	BiDir	GPIO SPI4W:Master, Chip Select, SPI_CSN SPI3W:Master, Chip Select, SPI_CSN
25	GPIO7	BiDir	GPIO SPI4W:Master, Data input, SPI_DI SPI3W:Master, Data IO, SPI_DIO I^2C:Data IO, I2C_SDA0
26	GPIO6	BiDir	GPIO SPI4W:Master, Clock output, SPI_CLK SPI3W:Master, Clock output, SPI_CLK I^2C:Clock output, I2C_SCL0
27	GPIO5	BiDir	GPIO SPI4W: Master, Data output, SPI_DO_1 I^2C:Data IO, I2C_SDA1 UART: UART_TXD0 (NOT for boot!)
28	GPIO4	BiDir	GPIO SPI4W: Master, Chip Select, SPI_CSN_1

Pin No.	Signal Name	Type	Description
			I^2C: Clock output, I2C_SCL1 UART: UART_RXD0 (NOT for boot!)
29	GPIO3	BiDir	GPIO SPI4W:Master, Data input, SPI_DI_1 UART: UART_RTS0
30	GPIO2	BiDir	GPIO, PWM0, or LED0 SPI4W: Master, Clock output, SPI_CLK_1 UART: UART_CTS0
31	GPIO1	BiDir	GPIO, PWM1, or LED1 Analog Input_1 I^2C:Data IO, I2C_SDA1 UART: UART_TXD1
32	GPIO0	BiDir	GPIO, PWM2, or LED2 Analog Input_0 I^2C: Clock output, I2C_SCL1 UART: UART_RXD0
33	DVDD15_BB	Power	Internal 1.5V LDO output for baseband, place a 1uF capacitor close to Pin33.
34	DVDD18_Flash	Power	Internal 1.8V LDO output for Flash, place a 1uF capacitor close to Pin4.
35	VDCDC	Power	DCDC output for internal LDOs.
36	LX	Power	Switch Node with connecting to inductor. Keep PCB trace as short and wide as possible.
37	PGND	Power	GND for DCDC
38	VBAT3V_P	Power	Buck mode: Input power pin, connector to battery or external power source. Recommend to add de-coupling cap, 10uF. Keep PCB trace as short and wide as possible.
39	VBAT3V	Power	Provide power for DCDC internal control unit. Keep PCB trace as short and wide as possible.
40	GND	GND	Connected to GND.
41	XTAL1_32k	In	Crystal input for 32.768kHz XTAL
42	XTAL2_32k	Out	Crystal output for 32.768kHz XTAL
43	RESETB	In	Active_L signal for HW reset. Recommended to add RC POR circuit (R=100k, C= 100nF) connected to VDDIO power domain.
44	AVDD2_BB	Power	Internal LDO input for baseband analog circuit, recommend to place a 0.1uF capacitor close to Pin44.
45	XTAL2	Out	Crystal output for 16MHz XTAL
46	XTAL1	In	Crystal input for 16MHz XTAL
47	AVDD2_SX	Power	Internal LDO input for RF_SX circuit, recommend to place a 0.1uF capacitor close to Pin47.
48	AVDD2_TRX	Power	Internal LDO input for RF_TRX circuit, recommend to place a 0.1uF capacitor close to Pin48.

*MUST use GPIO26 27f for boot. Cannot download code to Flash if GPIO4&5 are used as UART!

*Reserve reset button on EVB, otherwise cannot download code to Flash.

Table 2. IO Mode Selection

GPIO_#	0	1	2	3	4	5
GPIO0	GPIO0	Analog Input 0		I2C_SCL1	UART_RXD1	PWM2/LED2
GPIO1	GPIO1	Analog Input 1		I2C_SDA1	UART_TXD1	PWM1/LED1
GPIO2	GPIO2	M_SPICK_1			UART_CTS0	PWM0/LED0
GPIO3	GPIO3	M_SPIDI_1			UART_RTS0	
GPIO4	GPIO4	M_SPICSN_1		I2C_SCL1	UART_RXD0	
GPIO5	GPIO5	M_SPIDO_1		I2C_SDA1	UART_TXD0	
GPIO6	GPIO6	M_SPICK_0	M_SPICK_0	I2C_SCL0		
GPIO7	GPIO7	M_SPIDI_0	M_SPI_IO_0	I2C_SDA0		
GPIO8	GPIO8	M_SPICSN_0	M_SPICSN_0			
GPIO9	GPIO9	M_SPIDO_0				
GPIO10	GPIO10					
GPIO11	GPIO11					
GPIO12	GPIO12					
GPIO13	GPIO13					
GPIO14	GPIO14					PWM2/LED2
GPIO15	GPIO15			I2C_SCL1		PWM1/LED1
GPIO16	GPIO16			I2C_SDA1		PWM0/LED0
GPIO17	GPIO17				UART_CTS0	PWM2/LED2
GPIO18	GPIO18				UART_RTS0	PWM1/LED1
GPIO19	GPIO19				UART_RXD0	PWM0/LED0
GPIO20	GPIO20				UART_TXD0	PWM2/LED2
GPIO21	GPIO21					PWM1/LED1
GPIO22	GPIO22			I2C_SCL1	UART_RXD1	
GPIO23	GPIO23			I2C_SDA1	UART_TXD1	
GPIO24	GPIO24				UART_CTS0	PWM2/LED2
GPIO25	GPIO25				UART_RTS0	PWM1/LED1
GPIO26	GPIO26			I2C_SCL0	UART_RXD0	PWM0/LED0
GPIO27	GPIO27			I2C_SDA0	UART_TXD0	PWM2/LED2
ICE - CLK	ICE - CLK					PWM1/LED1
ICE - SDA	ICE - SDA					PWM0/LED0

3.0 Operating Specifications

3.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
VBAT3V Voltage	V_{BAT3V}	-0.4	V_{BAT3V}+0.3	V	
I/O Voltage	V_{DDIO}	-0.4	V_{DDIO}+0.3	V	
Relative Humidity	RH	0	50	%	Non-condensing, Non-biased
ESD	ESD_{HBM}		2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval.

Notes:
1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.
4. Functional operation under absolute maximum-rated conditions is not implied and should be restricted to the Recommended Operating Conditions.

3.2 Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature	T_A	-40	25	85	°C	
Operating Junction Temperature	T_J	-40	-	85	°C	
Power Supply Voltage for Buck DCDC converter	V_{BAT3V}	1.9	3.3	-	V	Buck DCDC Power input supply. Includes ripples
I/O Supply Voltage	V_{DDIO}	1.8	3.3	-	V	Includes ripples
Power Regulator Output Voltage	V_{DVDD15_BB}	1.4	1.5	1.65	V	Power for internal digital circuit
	V_{DVDD18_Flash}	1.7	1.8	2.1	V	Power for internal flash
Serial Clock Frequency	SPI_CLK	-	-	2	MHz	
	I2C_SCL	-	400[1]	1000[2]	KHz	

Note: SYD does not guarantee the performance if the operating temperature is beyond the specified limit.

3.3 Thermal Specifications

Table 5. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-40	-	125	°C	
Lead-free Solder Temperature	T_P	-	-	245	°C	Refer to Package Handling Information document

3.4 DC Characteristics

Table 6. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCDC Converter Input Voltage	V_{BAT3V}	1.8	3.3	-	V	
DCDC Converter Output Voltage	V_{Buck_OUT}	1.8	3.3	-	V	
DCDC Converter Output Current	I_{Buck_Out}	-	-	40	mA	Max current w/i keep setting output voltage
DCDC Converter Output Ripple	R_{Buck}	-	30	-	mV	Max. Ripple on DCDC converter output (Peak to Peak)
Power Consumption[2]						
TX RF Current @Pout = 0dBm			7.1		mA	@V_{BAT3V} = 3V with DCDC Buck enable
RX RF Current @sensitivity level			8.2		mA	@V_{BAT3V} = 3V with DCDC Buck enable
Supply Current @ Sleep	I_{SLEEP}	-	7.6	-	µA	@V_{BAT3V} = 3V with DCDC Buck enable
Supply Current @ Deep sleep	I_{PD}	-	2.5	-	µA	@V_{BAT3V} = 3V with DCDC Buck enable

Notes:

1. Electrical Characteristics are defined under recommended operating conditions.
2. All the parameters are tested under operating conditions: V_{BAT3V} = 3.0V, DCDC Buck enable mode at T_A = 25°C

3.5 AC and Timing Characteristics

3.5.1 16MHz Crystal Oscillator

The 16MHz Pierce crystal oscillator is designed for low power consumption and high stability. The 16MHz oscillator can be trimmed without external capacitors. Two digital controlled trimming loading capacitors are integrated and optimally designed for 9pF XTAL. Digital controlled capacitors could ease and speed up tuning procedure of XTAL frequency accuracy. The simplified schematic of the 16MHz crystal is shown in Figure 3.

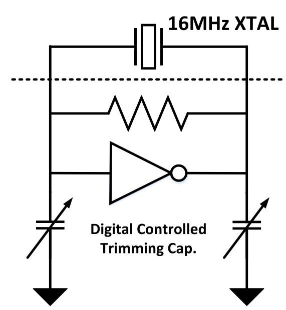


Figure 3. 16MHz Crystal Oscillator Circuit

Table 7. 16MHz Crystal Oscillator Specifications

Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Crystal Oscillator Frequency	F_{X16M}	-	16		MHz	
Crystal Oscillator Frequency tolerance	F_{X16M_TOL}	-	± 20	± 40	ppm	Frequency tolerance depends on XTAL Spec.
Equivalent series Resistor	ESR_{X16M}		30	100	Ω	
Loading Capacitor	C_{L_X16M}		9		pF	Built in digital controlled trimming loading cap, no external cap needed.
XTAL Drive Power	P_{DRIVE_X16M}			100	uW	
XTAL Start Up Time	T_{START_X16M}		0.4	1	ms	

Notes: Electrical Characteristics are defined under recommended operating conditions

3.5.2 32.768kHz Crystal Oscillator

The 32.768 kHz oscillator is designed optimally for XTAL with C-Load =12pF, and no internal trimming capabilities and 32.768kHz clock is used as the clock source in the Sleep or Power Down modes.

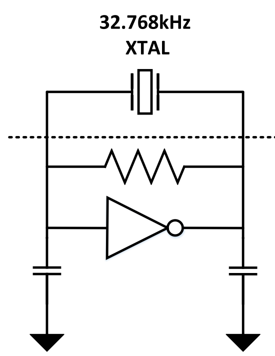


Figure 4. 32.768kHz Crystal Oscillator Circuit

Table 8. 32.768kHz Crystal Oscillator Specifications

Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Crystal Oscillator Frequency	F_{X32k}		32.768		kHz	
Crystal Oscillator Frequency tolerance	F_{X32k_TOL}		± 20		ppm	Frequency tolerance depends on XTAL Spec.
Equivalent series Resistor	ESR_{X32k}		50	80	kΩ	
Load Capacitor	C_{L_X32k}		12		pF	Built internal fixed load cap for 12pF XTAL
XTAL Drive Power	P_{DRIVE_X32k}			1	uW	
XTAL Start Up Time	T_{START_X32k}		0.3	1	s	

3.5.3 32MHz RC Oscillator

The 32MHz RC oscillator is designed for high speed wake up and high computing power application. Due to characteristic of RC oscillator, calibration is needed before switching to 32MHz RC oscillator mode.

Table 9. 32MHz RC Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Oscillator Frequency	F_{RC32M}		32		MHz	
RC Oscillator Frequency tolerance	F_{RC32M_TOL}		±1	±5	%	Calibration needed before switching to RC oscillator mode
Oscillator Start Up Time	T_{ST_RC32M}		2.5		us	

Notes: Electrical Characteristics are defined under recommended operating conditions

3.5.4 32.768kHzRC Oscillator

The 32.768kHz RC oscillator is designed for low cost applications without additional 32.768kHz XTAL. Due to characteristic of RC oscillator, calibration is needed before switching to 32.768kHz RC oscillator mode.

Table 10. 32.768kHz RC Oscillator Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
RC Oscillator Frequency	F_{RC32k}		32.768		kHz	
RC Oscillator Frequency tolerance	F_{RC32k_TOL}		±2		%	
RC Oscillator Frequency tolerance, Calibrated	F_{RC32k_TOL}		±250	±500	ppm	Calibration needed before switching to RC oscillator mode
Start Up Time	T_{START_X16M}		100		us	

Notes: Electrical Characteristics are defined under recommended operating conditions

3.6 RF Specifications

3.6.1 Transmitter RF Specification

Table 11. Transmitter Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Range	FR_{TX}	2402	-	2480	MHz	
Max. Output Power	$P_{O,MAX}$	-		4	dBm	
Default Output Power	$P_{O,DEF}$		0		dBm	
Output Power Adjust Range	$P_{O,ADJ}$	-30		4	dBm	
Output Power Variation	$P_{O,VAR}$		2.0		dBm	All channels TX power variation
TX 20dB Bandwidth	BW_{20dB}			1150	kHz	
1st Adjacent Channel Power	P_{AJC1}			-20	dBc	
2nd Adjacent Channel Power	P_{AJC2}			-40	dBc	
Delta F1 Frequency Deviation	$\Delta f1_{AVG}$	225		275	kHz	
Delta F2 Frequency Deviation	$\Delta f2_{AVG}$	185			kHz	
AVG Delta F2/ Delta F1	Δf_{AVG}	0.8				Δf2AVG/Δf1AVG
Frequency Offset	F_{OFFSET}	-150		150	kHz	
Carrier Frequency Drift	CF_{DRIFT}			50	kHz	
Carrier Frequency Drift rate	CF_{DRIFT_Rate}			20	kHz/50μs	
2nd Harmonics Power Level	Har_{2nd}			-40	dBm	@Pout = 0dBm

3rd Harmonics Power Level	Har_{3rd}			-45	dBm	@Pout = 0dBm

Notes: Electrical Characteristics are measured under BLE specification and recommended operating conditions

3.6.2 Receiver RF Specification

Table 12. Receiver Specifications

Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Frequency Range	FR_{RX}	2402		2480	MHz	
Maximum Input Power	RX_{MAX}		0		dBm	With PER <30.8%
Ideal Signal Sensitivity	SEN_{IDEAL}		-94	-93	dBm	All channels
Dirty Signal Sensitivity	SEN_{DIRTY}		-91	-90	dBm	All channels
C/I and Selectivity						
C/I Co-Channel	C/I_{CO}		9		dB	
C/I Adjacent +1MHz	C/I_{1M}		-1		dB	
C/I Adjacent +2MHz	C/I_{2M}		-35		dB	
C/I Adjacent≧ +3MHz	C/I_{3M}	-40	-48		dB	
C/I Image Channel	C/I_{IMG}		-25		dB	
C/I Image+1M Channel	C/I_{IMG+1M}		-35		dB	
Inter-Modulation Performance						
IMD performance	IMD		-24		dBm	3rd, 4th and 5th offset channel
Blocking Performance						
Blocking 30~2000MHz	$P_{BLK\_30\sim2000MHz}$	-10			dBm	
Blocking 2003~2399MHz	$P_{BLK\_2003\sim2399MHz}$	-30			dBm	
Blocking 2484~2497MHz	$P_{BLK\_2484\sim2497MHz}$	-30			dBm	
Blocking 3000MHz~12.75GHz	$P_{BLK\_3\sim12.75GHz}$	-10			dBm	

Notes: Electrical Characteristics are measured under BLE specification and recommended operating conditions

4.0 Design References

4.1 Application Schematics

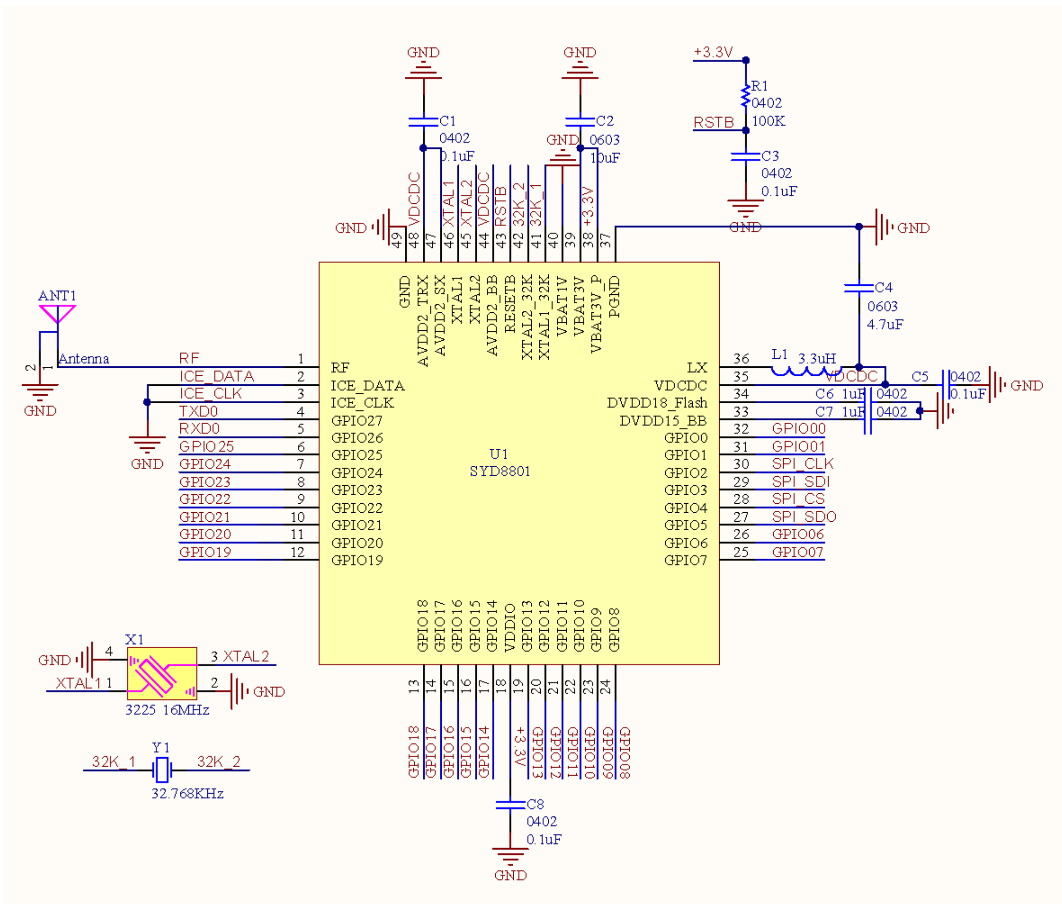


Figure 5. Reference Application Circuit （UART transmission）

4.2 Layout Design Guidelines

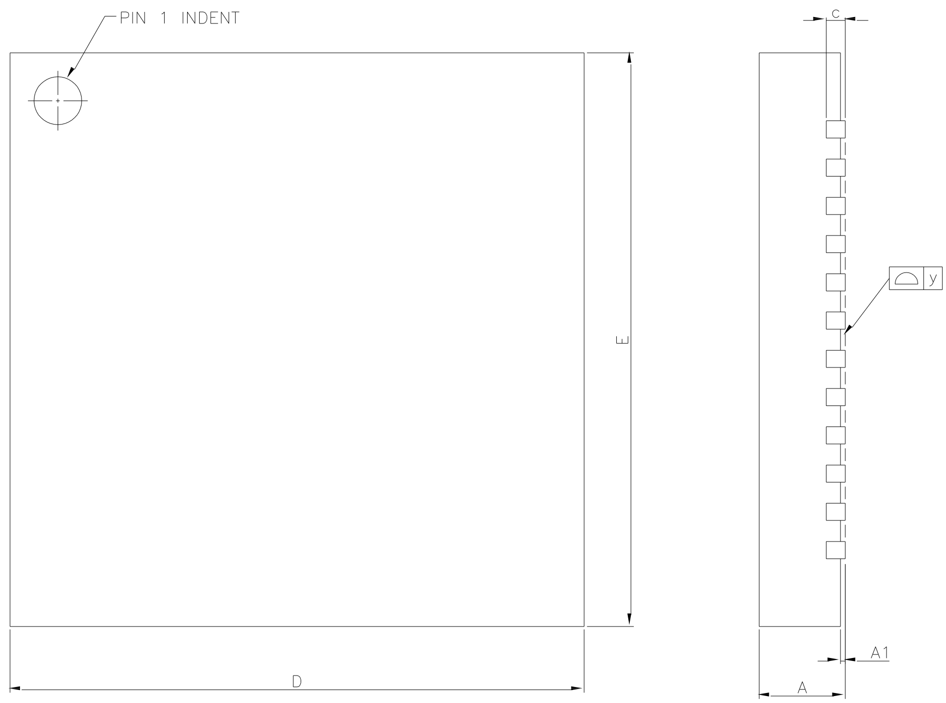
Precaution: PCB layout is extremely important to minimize parasitical capacitance and line inductance.
The following layout guidelines are recommended to achieve optimum performance.

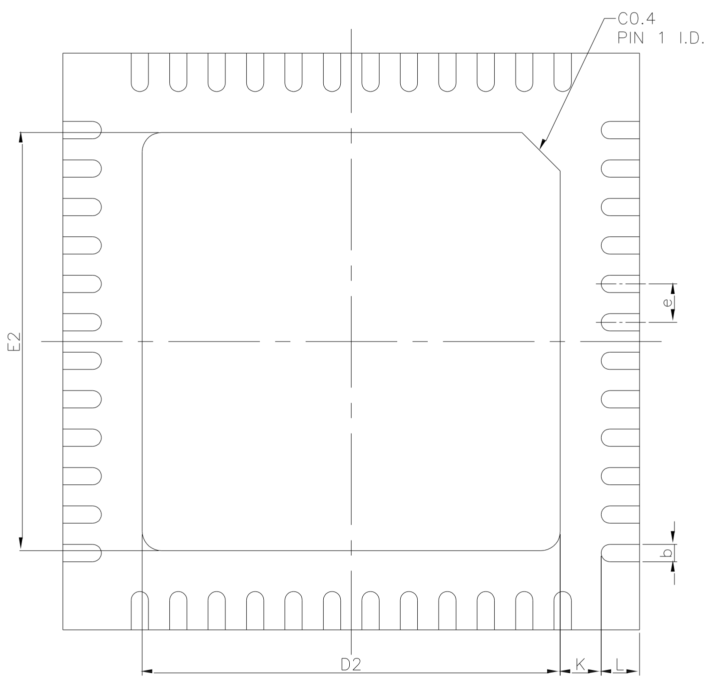
1. Make sure RF 50-ohm trace is with GND continuation.
2. Place the buck converter inductor close to the LX pin. Keep the traces short, direct, and wide.
3. Place bypass capacitors near the input/output pins.
4. Star connection for VBAT3Vand VBAT3V_P, place 10uF C2 near VBAT3V_P, 0.1uF C9 near VBAT3V;
5. Route PIN37 PGND to gnd plane by VIA（4layer PCB）, or Route PGND to bottom layer by VIA (2layer PCB), DO NOT connect PGND to top layer gnd; **PGND is dirty DCDC gnd.
6. Connect PIN49 GND to top layer GND though the three corners (except PGND corner), and connect to bottom layer GND by 9 VIAs;

7. All feedback signals must go through the regulator capacitors first.
8. Place the crystal and its components close to the oscillator side and near the oscillator pins.
9. Ensure that the ground plane under the oscillator and its components are in good quality.
10. Avoid long connections to the crystal and also to the load capacitor which may create a large loop on the PCB.
11. Do not route any digital-signal lines on the opposite side of the PCB under the RF trace and crystal area.
12. Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from crystal/analog/RF connections as possible.
13. Place at least 9 ground vias directly under IC thermal PAD for good grounding and thermal dissipation.

5.0 Mechanical Specifications

5.1 Mechanical Dimension





SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	---	0.20 REF.	---
D	5.90	6.00	6.10
D2	4.30	4.35	4.40
E	5.90	6.00	6.10
E2	4.30	4.35	4.40
e	---	0.40	---
K	---	0.425 REF.	---
L	0.350	0.400	0.450
y	0.00	---	0.075

Figure 6. Package Outline Diagram and Dimension

5.2 Package Marking

Refer to Figure 7 for the code marking location on the device package.

Figure 7. Package Marking

Table 13. Code Identification

Marking	Description
LYWWXXXX	SYD Date Code Y: Assembly year e.g. (Yearly 2016) -> 6 WW: Assembly week e.g. (Weekly 53) -> 53 XXXXX: NO. e.g. 433CE

6.0 Power States & Sequence

6.1 Operation Mode

State	Functional Description
Deep sleep	All power supplies are off except I/O for pin wake-up. All clocks are gated. System can be woken up by configured external pin. When it happens, SYD8801 resets from boot-up state.
Sleep	Active clocks (16MHz or 32MHz) are off, and the sleep clock (32.768kHz) remain working. Certain engines' power are off. Two types of sleep modes are provided in SYD8801. When CPU uses 16MHz crystal clock together with Bluetooth, it follows Bluetooth sleep mode aligning to connection interval. When CPU uses internal 32MHz RC clock, it can set CPU sleep mode independently and woken up by timer or Bluetooth interrupts.
Standby	This is the default state after power-up. All clocks are working but the RF is inactive.
TX	This mode is entered when Bluetooth link-layer determines to send transmission packets.
RX	This mode is entered when Bluetooth link-layer determines to receive an incoming packet.

7.0 System Description

7.1 ARM Cortes M0

The ARM® Cortex®-M0 processor is the smallest ARM processor available. It provides low power consumption and minimal code of the processor to enable developers to achieve 32-bit performance. With its friendly architecture, users can develop applications easily and fast.

SYD8801 supports dynamic clock technology for various applications ranging from 8MHz to 32MHz. The CPU clock can be configured to use internal 32MHz RC clock or 16MHz crystal clock. When using RC clock, MCU can run independently with Bluetooth link-layer and switch on and off at users' discretion. When using 16MHz crystal clock, it should follow the working period of Bluetooth. However, the Bluetooth working period can be determined by MCU.

SWD (Serial-Wire Debug) is supported for powerful debug and trace features with two connection pins.

SYD8801 has 24kB ROM for boot-up and BLE protocol stack, 128kB flash for profile/application, 48kB internal program SRAM, and 32kB data SRAM.

7.2 Memory

- ROM: 24kB internal ROM is for the Boot code and Bluetooth Low Energy protocol stack firmware.
- Code RAM (PRAM): 48kB Code RAM is reserved for programming code loaded from flash. All 48kB is available for application
  - 0x0000 0000 ~ 0x0000 6000 (24kB) is ROM Code address.
  - 0x0000 6000 ~ 0x0001 2000 (48kB) is Application Code address.
- Data RAM: 32kB Data RAM is storing data contents. For Data RAM, 3kB will be used up by ROM, only 29kB is available for application.
  - 0x2000 0000 ~ 0x2000 0C00 (3kB) is used by ROM.
  - 0x2000 0C00 ~ 0x2000 8000 (29kB) is available for application
- Flash: 128kB SPI flash is integrated for firmware and data storage.

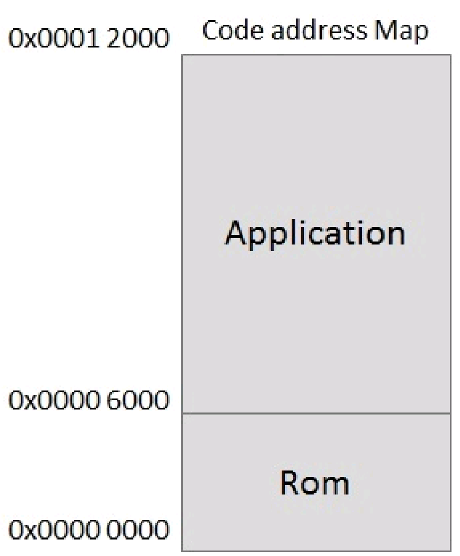


Figure 8. Code RAM Address Mapping

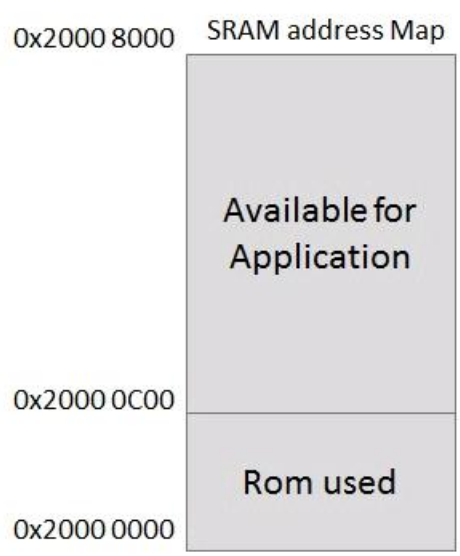


Figure 9. Data RAM Address Mapping

7.3 Bluetooth Low Energy Core

The Bluetooth Low Energy Core is SIG Qualified. It is fully compliant with Bluetooth Smart v4.0 slave-role controller and provides qualified features as below:

- Bluetooth low energy stack: All layers up to GATT including (PHY, LL, HCI, L2CAP, GAP, SM, ATT/GATT)
- Slave-Role Link layer
  - Slave-required PDU types
  - Encryption/Decryption
- L2CAP
  - Slave connection update
  - Attribute channel
  - Security channel
- GAP/ATT/GATT: Mandatory protocols
- Security Management
  - Key generation and passing
  - Automatic security engine
- DTM: For RF qualification
- Profile configuration
  - Initialization
  - Flexibility and testability

7.4 Radio Transceiver

The SYD8801 integrates high performance 2.4GHz radio transceiver for Bluetooth radio specification. With the built-in on-chip balun, SYD8801 does not need external balun circuit to minimize BOM. The integrated high efficiency PA can transmit up to +4dBm RF power for class 2 operation, while the integrated low-IF receiver can provide excellent sensitivity up to -93dBm and outstanding interference rejection capability.

7.5 General Purpose ADC

The SYD8801 integrates a low power 10-bit general purpose Analog-to-Digital Converter (GPADC) with 32kHz sampling rate. For each one shot measurement, it takes 150us for data acquisition. It can operate as a 4-channel ADC by switching the GPADC input. Two channels for internal Battery Voltage detection (V_{BAT3V}, V_{BAT1V}), while the other two are configured to monitor GPIO0 or GPIO1. For better accuracy, internal reference voltage calibration is preferred. Sensing applications as battery monitoring, temperature resister, analog signal sampling could be applied with this GPADC.

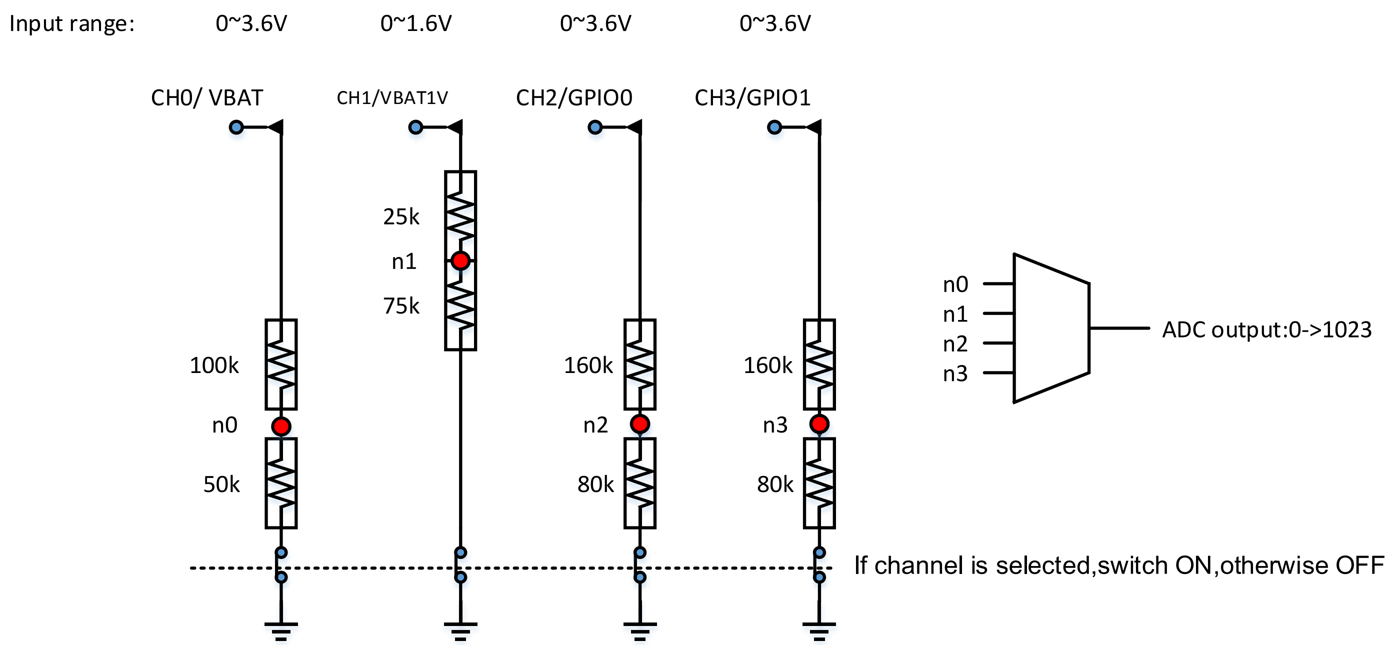


Figure 10. GPADC Internal Channel MUX and Resister Divider Configuration

7.6 Power Management

The SYD8801 integrates a power management unit for handheld or wearable devices with DCDC converter. No external Schottky diode is needed for minimal layout area. The DCDC converter transforms battery voltage to a lower/higher internal voltage with minimal power loss. The DCDC converter could provide excellent power efficiency with adaptive loading current setting. The DCDC Buck converter can be bypassed when the supply voltage drops to the lower limit of the voltage range, and external DCDC converter is also supported. It can provide power solution for one-cell Lithium-Ion, one-cell or two serial alkaline battery applications where the output voltage is adjustable, 1.8V~3.3V.

7.6.1 Buck Converter

Higher performance DCDC Buck converter would bring up better battery life time. To ensure longest battery life, Buck converter has an optional bypass mode under light load current. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. For better conversion efficiency, DC resistance (R_{DC}) should be less than 0.25ohm.

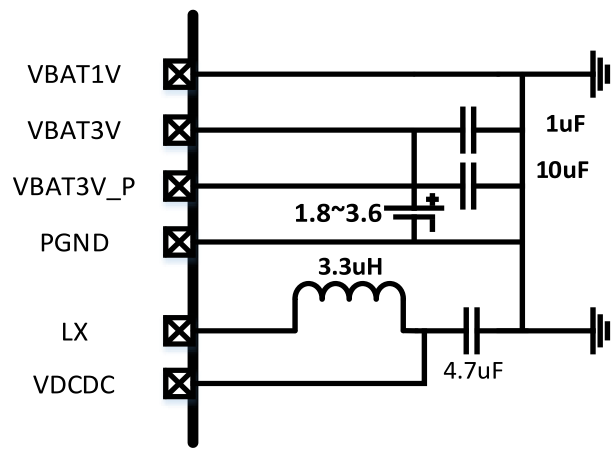


Figure 11. DCDC Buck Converter Configuration

Table 14. Buck Converter Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Voltage	$V_{In,Buck}$	1.8	3.3		V	
Output Voltage	$V_{DCDC,Buck}$	1.8	3.3		V	
Converting Efficiency	Eff_{Buck}		88		%	@20mA Loading current
Maximum Load Current	$I_{Load,Buck}$			40	mA	
Output Ripple Voltage	$V_{RIPPLE,Buck}$		30		mV	

7.6.2 GPIO

SYD8801 offer 28 GPIOs and 2 output only ports (ICE_CLK, ICE_DATA). ICE_CLK and ICE_DATA pins should be make sure that keep Low during SYD8801 booting procedure. ICE_CLK and ICE_DATA could be configured as output pin after system boot up.

7.6.3 Timer

SYD8801 provide 4 timers with 32-bit width. Timer0~Timer3 are running with 32.768kHz clock from 32.768kHz XTAL or LPO. Timer interrupt can wakeup CPU from sleep or power down mode. Timer3 is reserved for Rom Code.

7.6.4 Watch Dog Timer (WDT)

SYD8801 offer one 16-bit countdown watchdog timer for supervisor purpose. It also runs at 32.768kHz clock for maximum 2sec supervisor time to execute system reset due to a hardware fault or program error.

7.6.5 PWM

SYD8801 integrates three adjustable PWM generators which are controlled by individual register and could be mux out at three different GPIOs. The minimum positive or negative width of PWM is 1/32ms and flexible setting ranges from 1 to 255 steps. Buzzer or LED dimming could be controlled by PWM signal with pre-defined PWM duty.

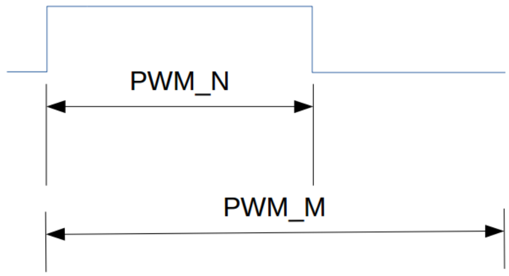


Figure 12. PWM Timing Setting Diagram

7.6.6 LED Controller

SYD8801 integrate LED controller which provide general On-OFF mode and Breathing light mode. The minimum LED on width is 1/32s with max 255 steps. LED ON-OFF repetition times could be configured as continuous or 1~127 times. Register table has setting description details. T1, T2, T3 are 8-bit width control register with minimum step 31.25ms.

For Breathing light mode, min, max, T4 are 8-bit width control register with minimum step 0.5ms. The sp is defined as breath mode speed with 4-bit width control resister with minimum step, 31.25us.

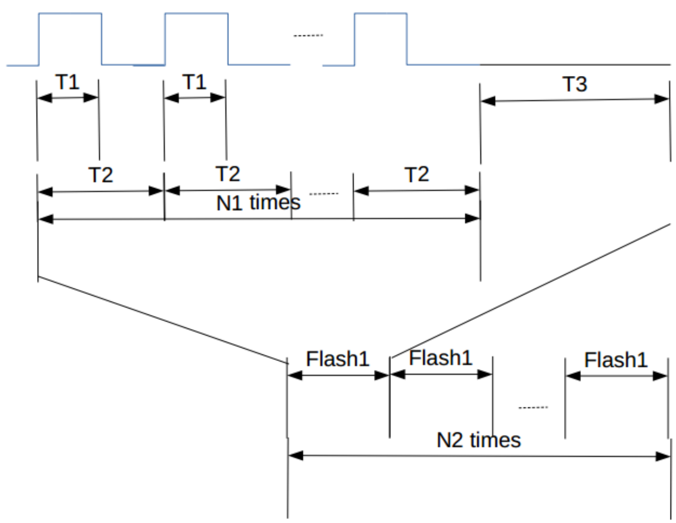


Figure 13. LED ON-OFF Setting Diagram

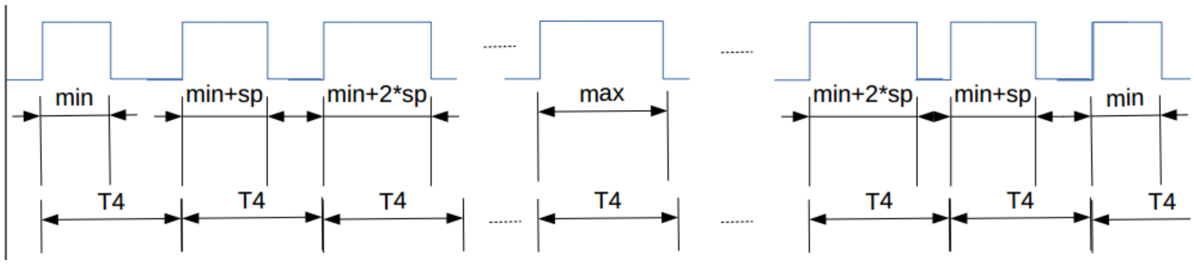


Figure 14. LED Breathing Light Setting Diagram

8.0 Interfaces

8.1 UART

The SYD8801 has two sets of UART interface (UART0, UART1) for serial asynchronous communication between devices.UART-0 has CTS/RTS hard flow control for option. 8-n-1 is standard data frame configuration as eight (8) data bits, no (N) parity bit, and one (1) stop bit shown figure below.

Figure 15. UART Data Frame

Table 15. UART Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Baud Rate	BR	1200		921600	bps	
Baud Rate Accuracy	BR_{ACCU}			3.0	%	

8.2 I2C

The SYD8801 has two sets of I2C interface (I2C_0, I2C_1) for 2-wire bi-directional communication between devices. The I2C supports wide range of data rate from 31.25kHz to 1000kHz in register controls. Multiple Read modes are supported as current read, random read, and sequential read. Write mode also support byte write and page write.

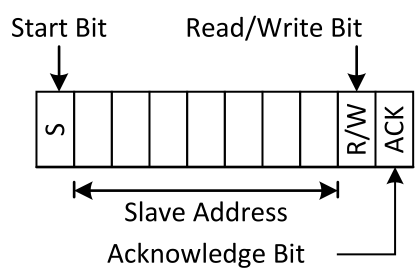


Figure 16. I2C Control Byte Format

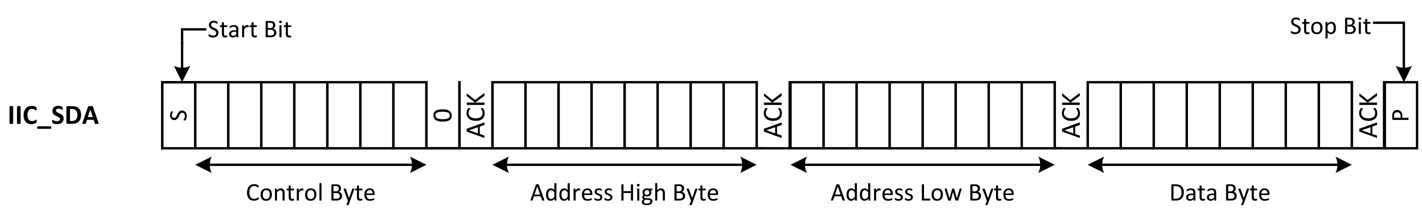


Figure 17. I2C Byte Write Format

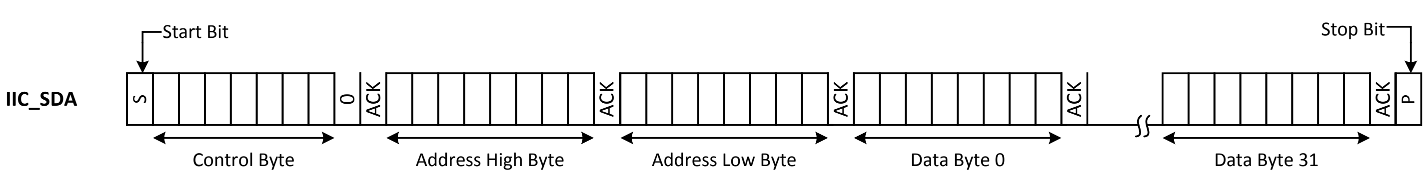


Figure 18. I2C Page Write Format

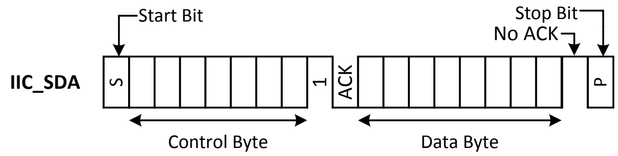


Figure 19. I2C Current Read Format

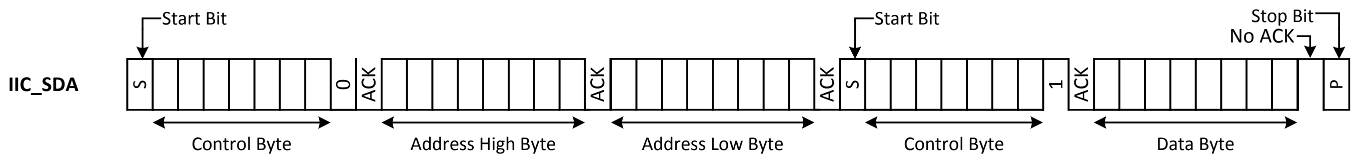


Figure 20. I2C Random Read Format

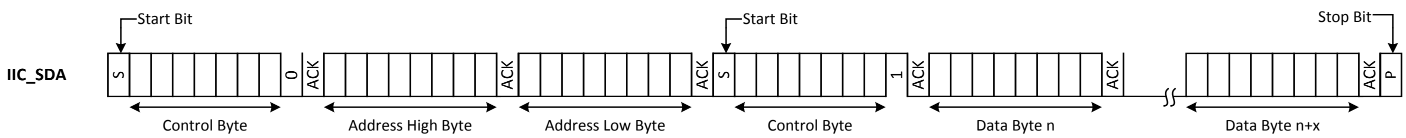


Figure 21. I2C Sequential Read Format

8.3 SPI

The SYD8801 provides two configurations of SPI interfaces. One is four wire SPI, as CSN (chip select), SCLK (clock), SDI (MOSI data) and SDO (MISO data)and the other is two or three wire SPI interface as CSN (chip select) – optional, SCLK (clock), SDIO (bi-directional Data). These two configurations are for master operation only, slave mode is not supported.

8.3.1 Packet Formats

The transmission protocol consists of the two operation modes:

- Write Operation.
- Read Operation.

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has bit-7 as its MSB to indicate data direction. The second byte contains the data.

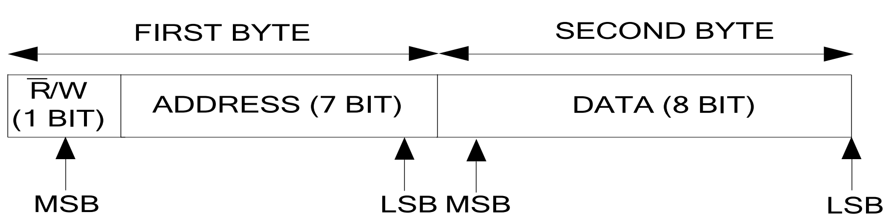


Figure 22. Four-wire or Three/Two-wire SPI Transmission Protocol

8.3.2 Write Operation

A write operation is always initiated by theSYD8801 and consists of two bytes, which the data is going from the host controller to the device. The first byte contains the 7 bits address and has a "1" as its MSB to indicate data direction. The second byte contains the full 8 bits data. The communication is synchronized by SCLK. The SYD8801 changes SDIO or SDI on the falling edges of SCLK and the device reads SDIO or SDI on the rising edges of SCLK.

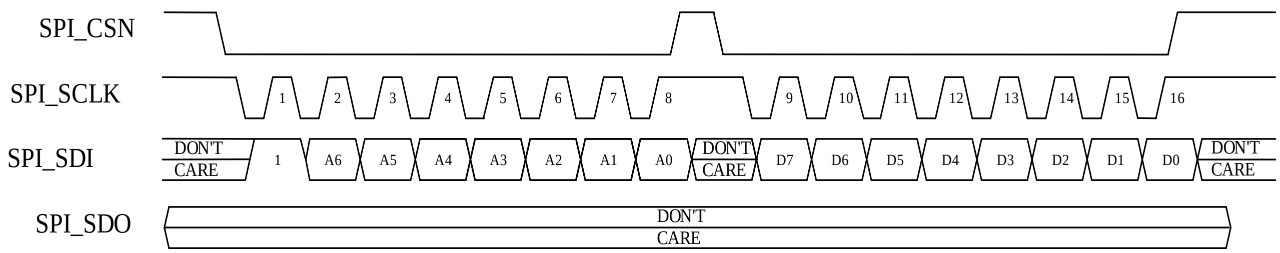


Figure 23. Four-wire SPI Write Operation

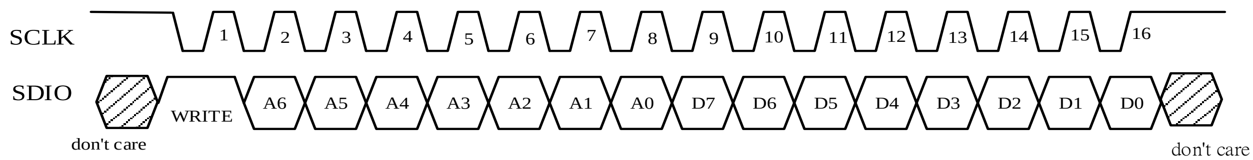


Figure 24. Three/Two-wire SPI Write Operation

8.3.3 Read Operation

A read operation is initiated by the host controller and consists of two bytes. The first byte contains 7-bit address specified by SYD8801 and has a "0" as its MSB to indicate data direction. The second byte contains the full 8 bits data and is driven by the slave device. This communication is synchronized by SPI_SCLK. For three/two-wire SPI, SDIO is changed on the falling edges of SCLK and is read on every rising edge of SCLK. SYD8801 release SDIO bus and handover the control of SDIO bus to the device on the falling edge of last address bit.

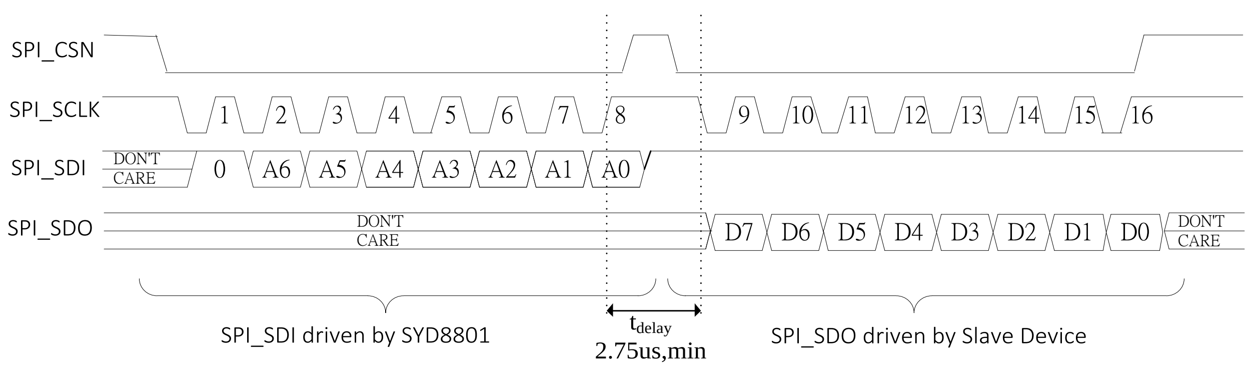


Figure 25. Four-wire SPI Read Operation

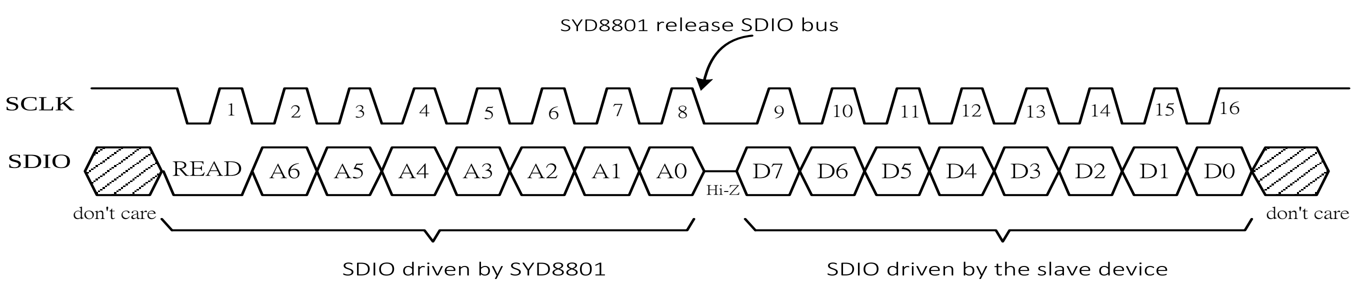


Figure 26. Three/Two-wire SPI Read Operation

Document Revision History

Revision Number	Date	Description
1.0	20 Feb 2016	1st version;
2.0	23 Sep 2016	2nd Version Correct typos; modify the reference layout rule;

SYD 官方网站： http://www.syd-tek.com

SYD 技术支持： http://bbs.syd-tek.com